2024 SEMICON WEST TECHNOLOGY BREAKFAST

Forward-Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

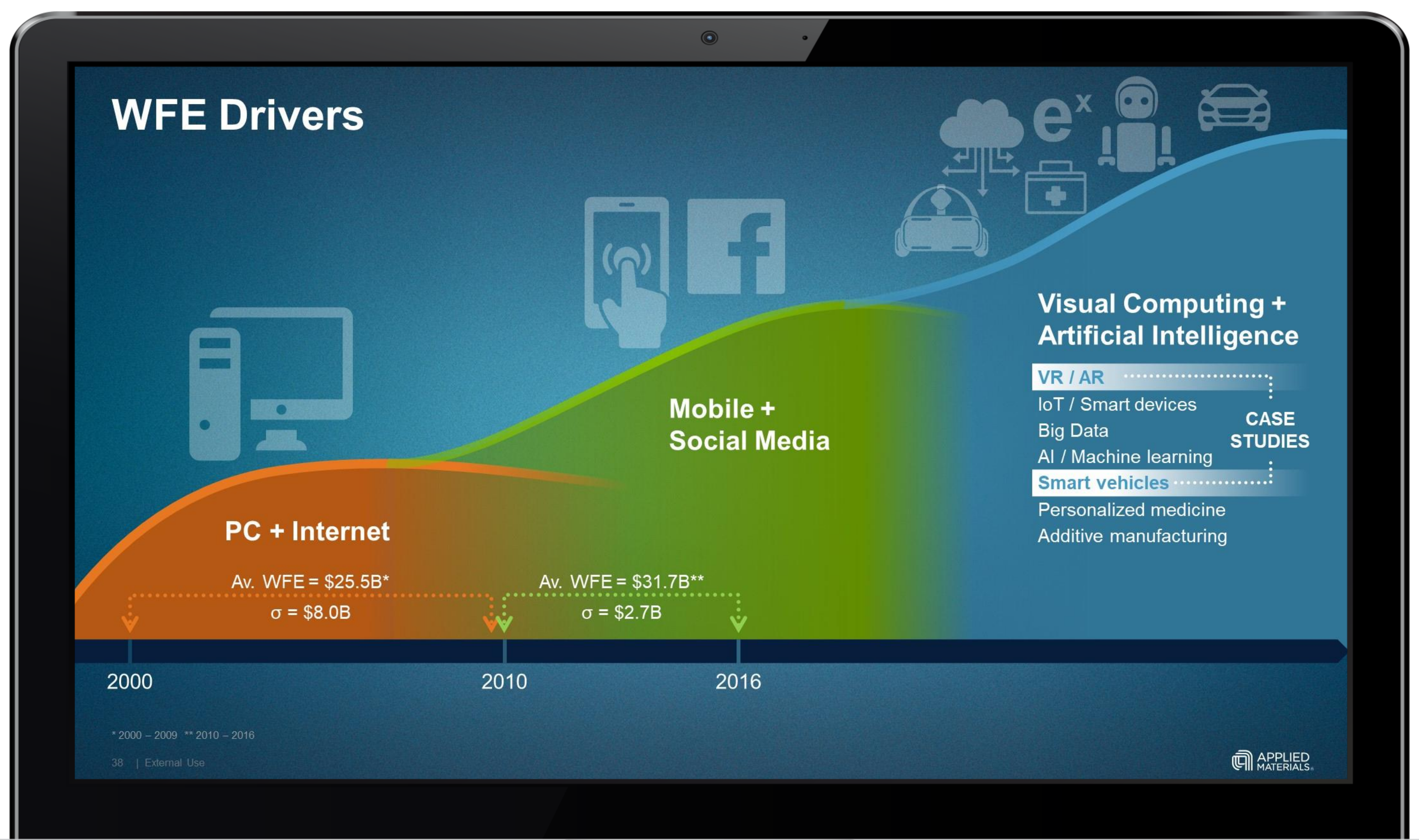
Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including rising inflation and interest rates; the implementation and interpretation of export regulations and license requirements, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies; our ability to obtain licenses or authorizations on a timely basis, if at all; the effects of geopolitical turmoil or conflicts; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of regional or global health epidemics; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

RACE FOR AI LEADERSHIP

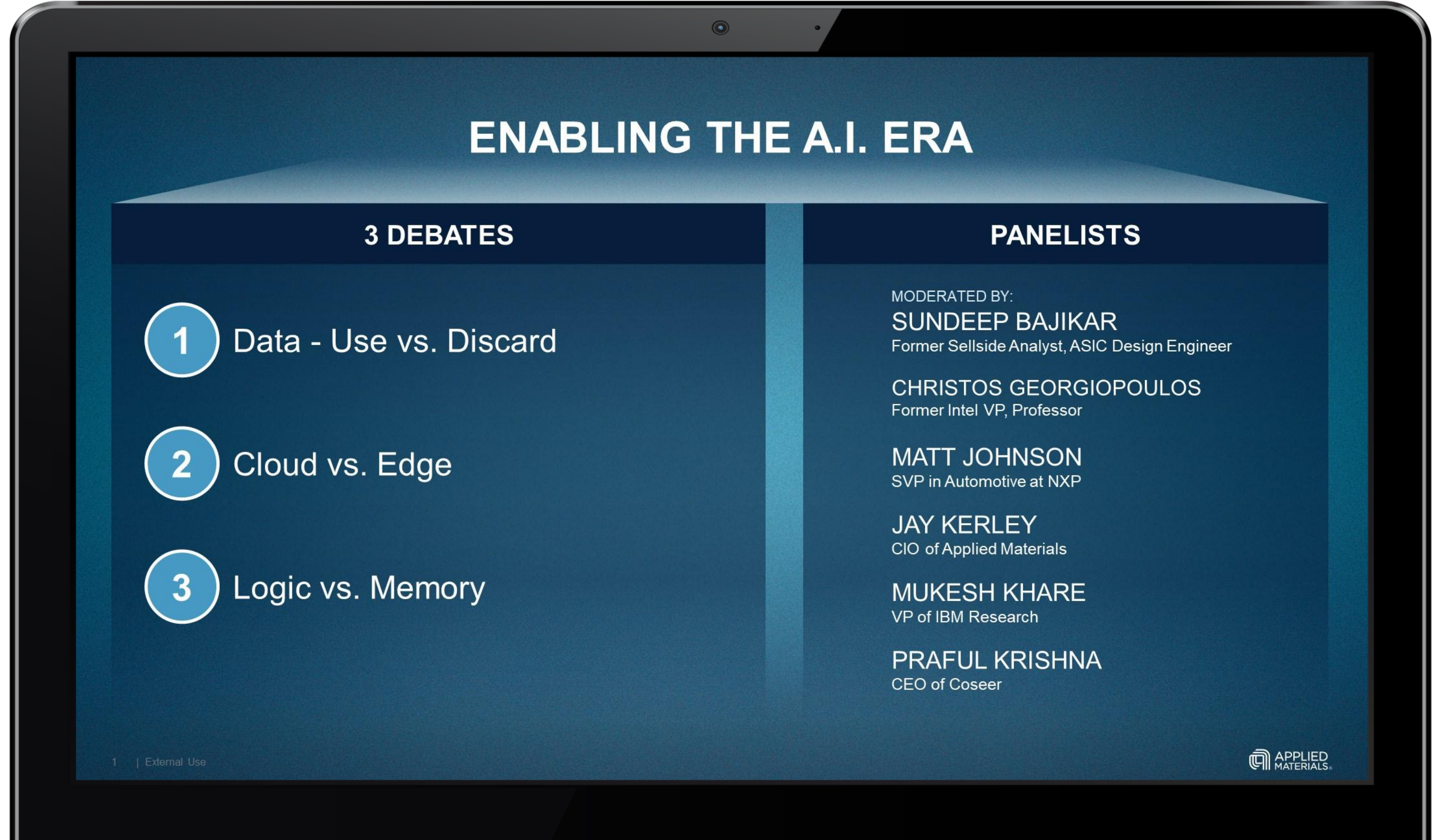
Fueled by Materials Engineering

Michael Sullivan
Corporate Vice President

JULY 9, 2024

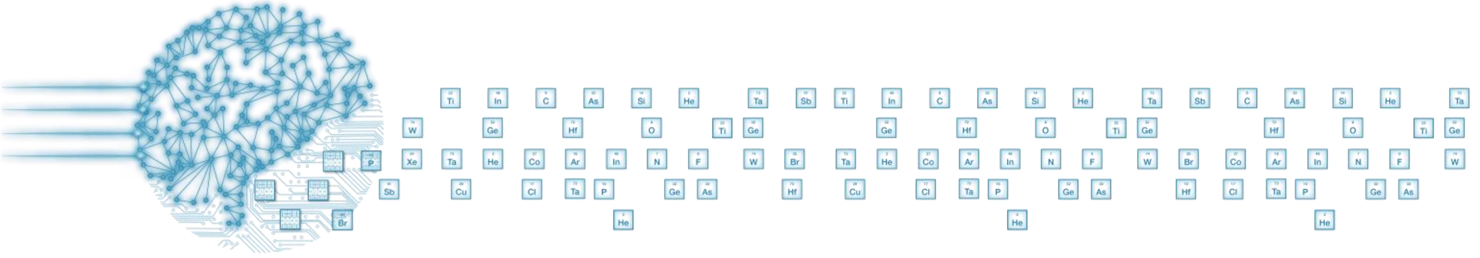


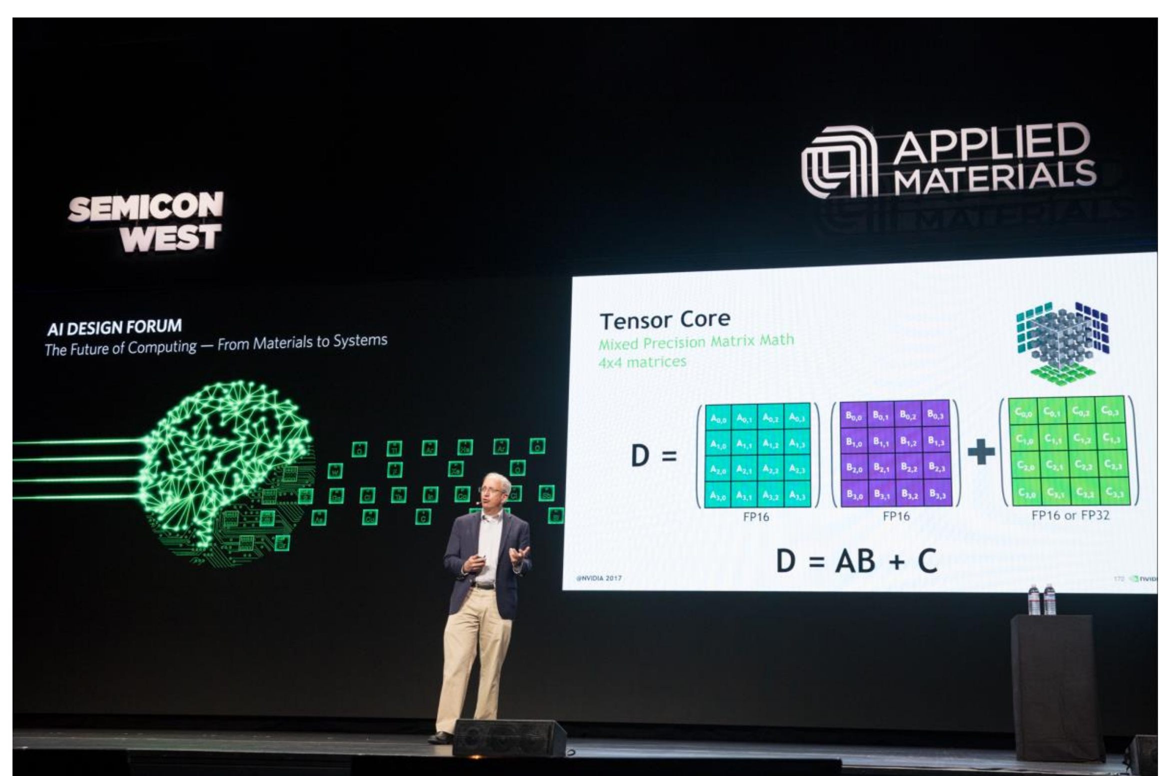
WFE Drivers
PC + Internet
Mobile +
Social Media
Visual Computing +
Artificial Intelligence
VR / AR
IoT / Smart devices
Big Data
AI / Machine learning
Smart vehicles
Personalized medicine
Additive manufacturing
CASE
STUDIES
Av. WFE = $25.5B*
σ = $8.0B
Av. WFE = $31.7B**
σ = $2.7B
2000
2010
2016
* 2000 – 2009 ** 2010 – 2016
38 | External Use
APPLIED MATERIALS


ENABLING THE A.I. ERA
3 DEBATES
1 Data - Use vs. Discard
2 Cloud vs. Edge
3 Logic vs. Memory
PANELISTS
MODERATED BY:
SUNDEEP BAJIKAR
Former Sellside Analyst, ASIC Design Engineer
CHRISTOS GEORGIOPOULOS
Former Intel VP, Professor
MATT JOHNSON
SVP in Automotive at NXP
JAY KERLEY
CIO of Applied Materials
MUKESH KHARE
VP of IBM Research
PRAFUL KRISHNA
CEO of Coseer
1 | External Use
APPLIED MATERIALS

AI Design Forum™ 2018

Tuesday, July 10, Yerba Buena Theater, SF

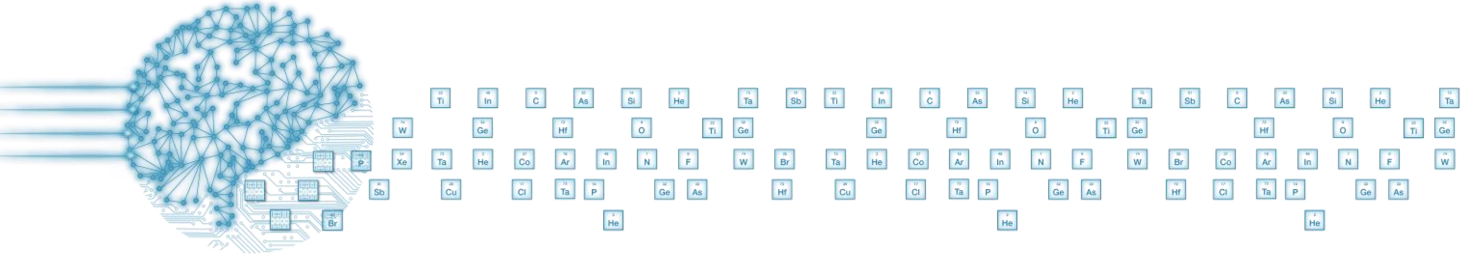




Bill Dally, Ph.D.
Chief Scientist
NVIDIA

AI Design Forum™ 2018

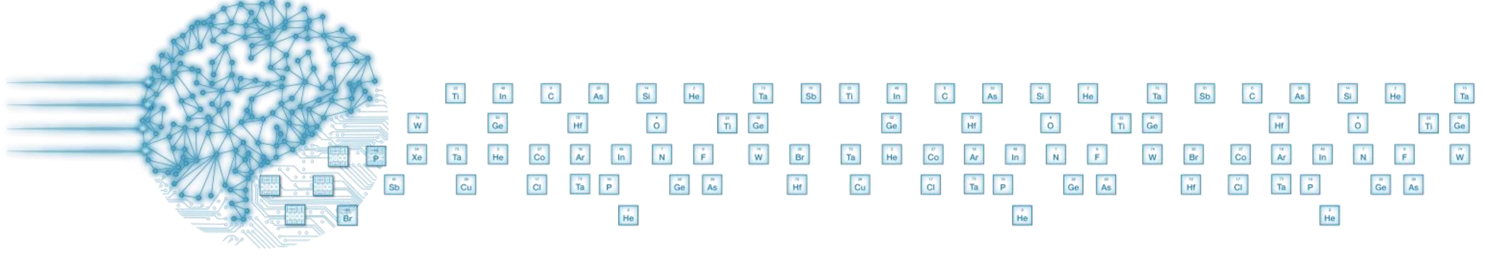
Tuesday, July 10, Yerba Buena Theater, SF

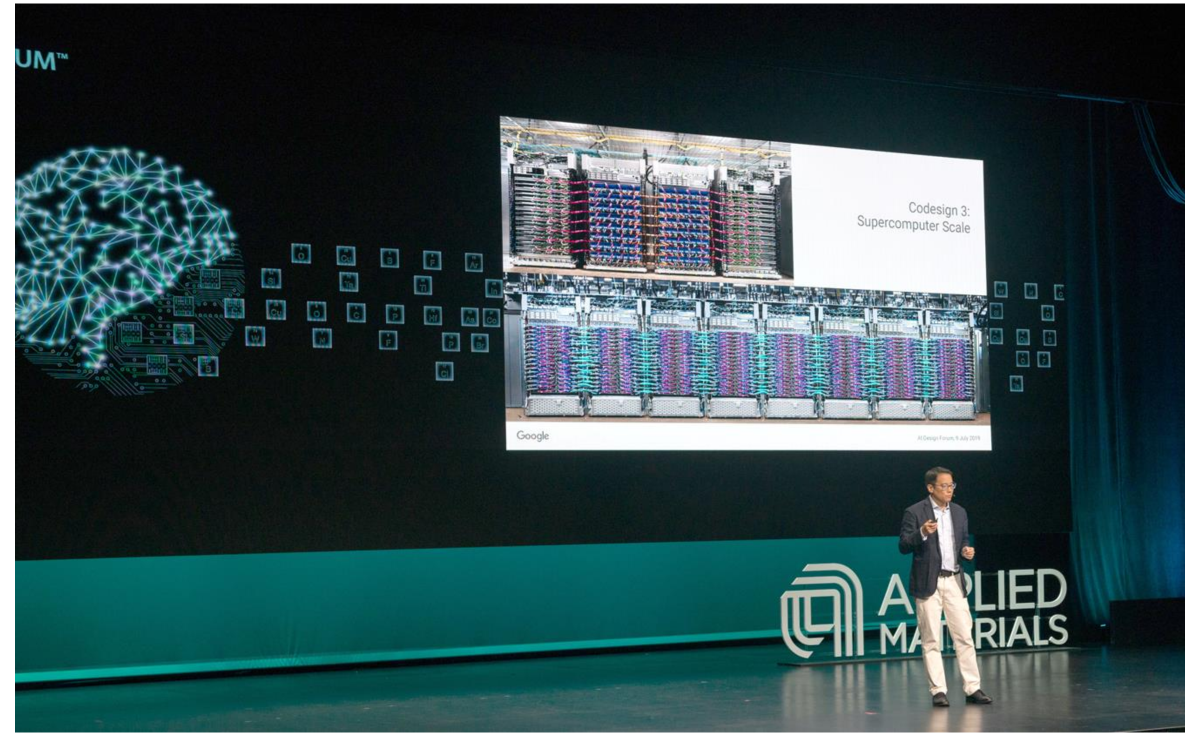


Gary Dickerson
CEO
Applied Materials

AI Design Forum™ 2019

Tuesday, July 9, Yerba Buena Theater, SF





Let's push from Google and the other AI people down towards materials. And let's push from materials and devices back up.

I'd love to learn about your field and teach you about my field so we can build those solutions and the next generation of TPUs together."

Cliff Young, Ph.D.
Software Engineer
Google

APPLIED MATERIALS

AGENDA

7:35 Prabu Raja, Ph.D.
Race for AI Leadership
Fueled by Materials Engineering

7:55 Mark Fuselier
Power and Performance in the AI Era

8:10 Mukund Srinivasan, Ph.D.
Enabling the AI Device Inflections

8:20 Device Inflection Expert Panel

- Mehul Naik, Ph.D. — Transistors and Wiring
- Sony Varghese, Ph.D. — DRAM
- Jinho An, Ph.D. — High-Bandwidth Memory
- Sarah Wozny, Ph.D. — Heterogeneous Integration

8:50 Prabu Raja, Ph.D.
Growing our Opportunity and Share

PRESENTATIONS ARE POSTED AT
https://ir.appliedmaterials.com/events

RACE FOR AI LEADERSHIP

Fueled by Materials Engineering

Prabu Raja, Ph.D.
President, Semiconductor Products Group

JULY 9, 2024

Tectonic Shifts in Technology are Built on Semiconductors

DATA CENTER AI

$8T
by 2030[1]

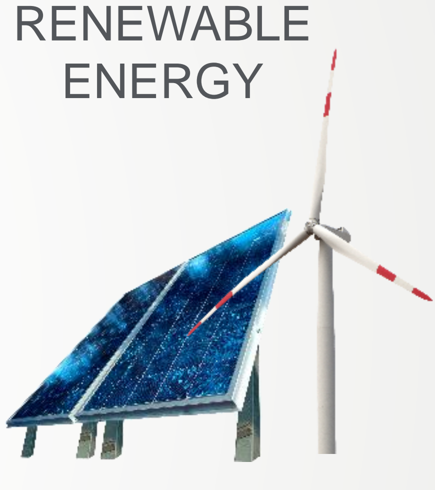
EDGE AI and IOT

$2T
by 2030[2]

EV and AV

$1.5T
by 2030[3]

RENEWABLE ENERGY



$4.5T
by 2030[4]

Source: 1 Gartner, 2 Fortune & Skyquest , 3 Yole, assumes 40% EV/AV L2+, 4 IEA

AI is the biggest inflection of our lifetimes

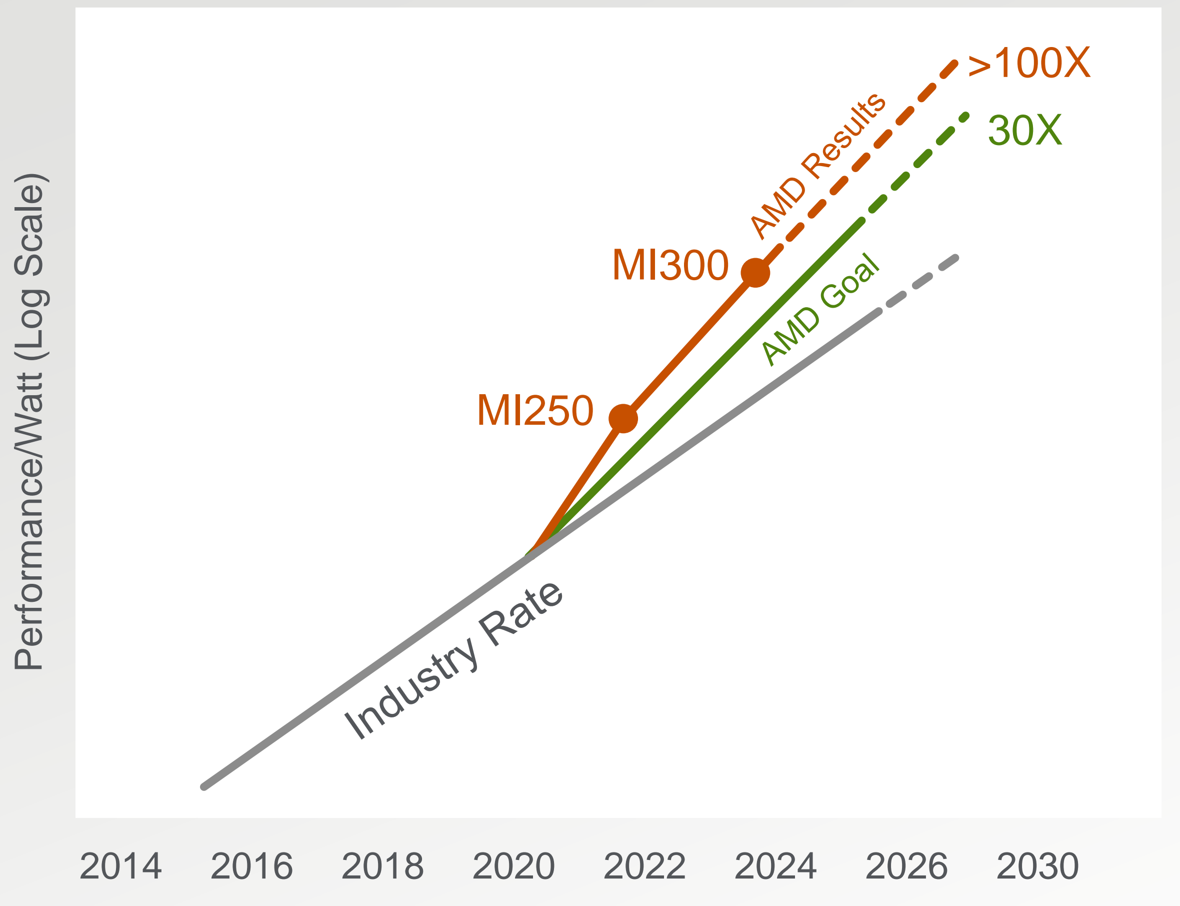
Growth in AI Driving Increasing Energy Consumption

	GPT-2 (2018)	GPT-3 (2020)	GPT-4 (2023)
Compute for Model Training (FLOPs)	1X	100X	10,000X
Energy Consumption[1]	1X	20X	250X
Number of Chips[2]	1X	20X	100X

AI to grow to 8% of US electricity demand[3] by 2030

Source: Generative AI 2024 - Impact on Processors, Memory, Advanced Packaging, and Substrates report, Yole Intelligence, 2024.
1 Four NVIDIA H100 for one CPU Intel Xeon Platinum, at 90% of MAX thermal dissipation power (TDP) and ~60% for other electronic components and cooling.
2 Number of NVIDIA H100 GPUs
3 Source: Goldman Sachs Global Investment Research, 2024

Industry Focused on Accelerating Energy-Efficient Performance



"Over the next decade, we must think of energy efficiency as the most important challenge."

Lisa Su, Ph.D.
CEO, AMD

Source: https://spectrum.ieee.org/amd-eyes-supercomputer-efficiency-gains and imec ITF World 2024

Key Architecture Inflections Fueling the AI Race

Leading-edge logic

High-performance DRAM

High-bandwidth memory

Advanced packaging

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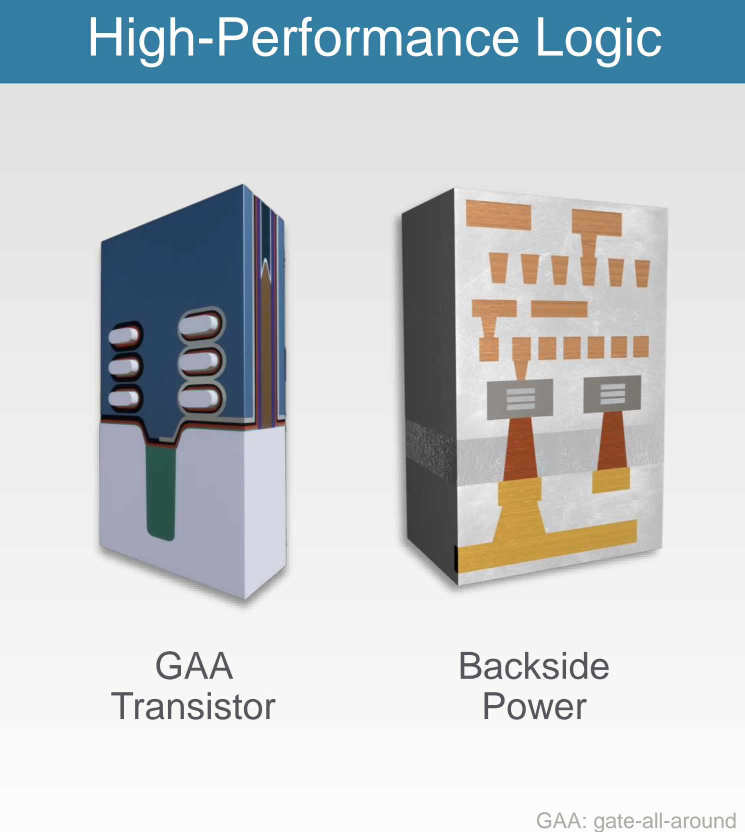
All Architecture Inflections Are Becoming 3D

High-Performance Logic

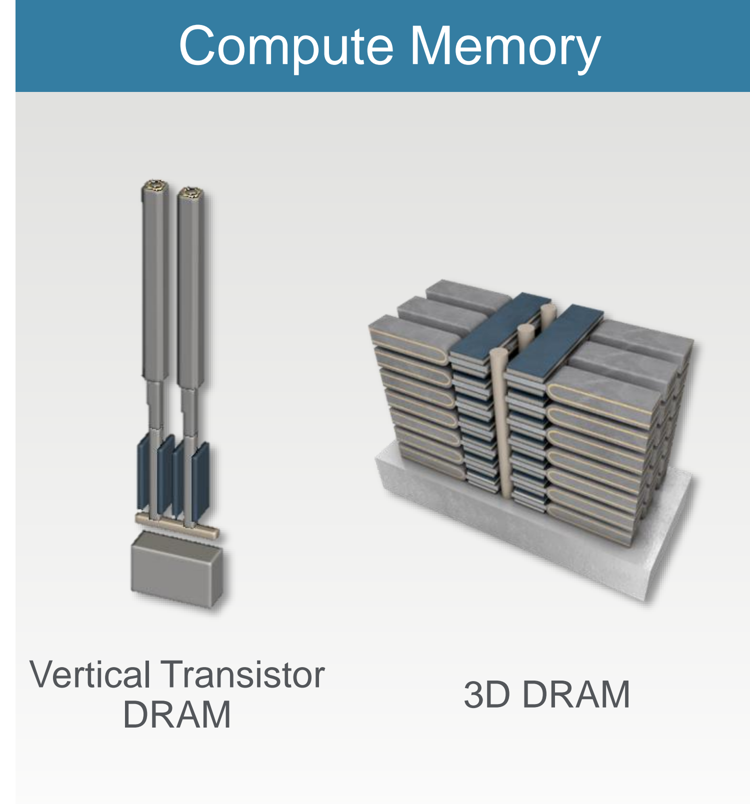


GAA Transistor

Backside Power

GAA: gate-all-around

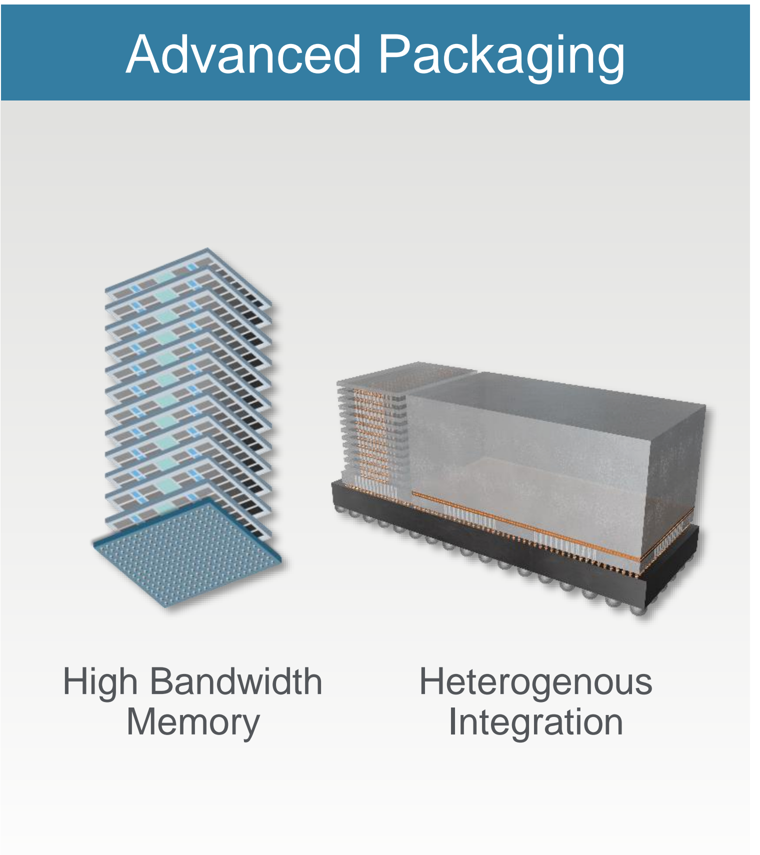
Compute Memory



Vertical Transistor DRAM

3D DRAM

Advanced Packaging



High Bandwidth Memory

Heterogenous Integration

Race to bring new architectures to market and secure AI leadership

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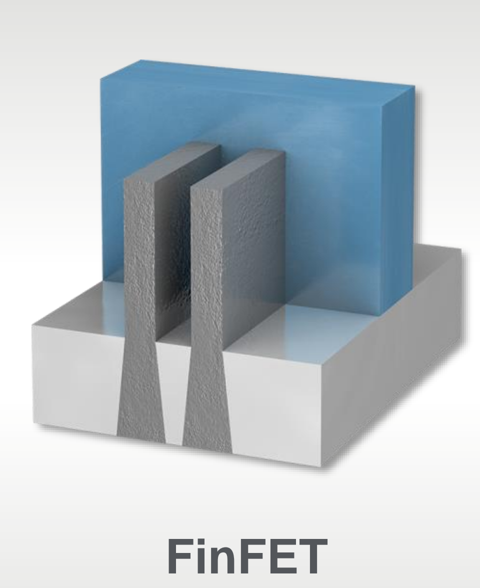
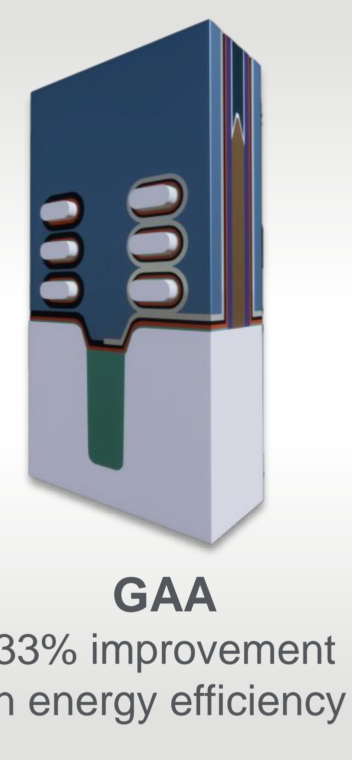
3D Inflections Have Increasing Process Complexity



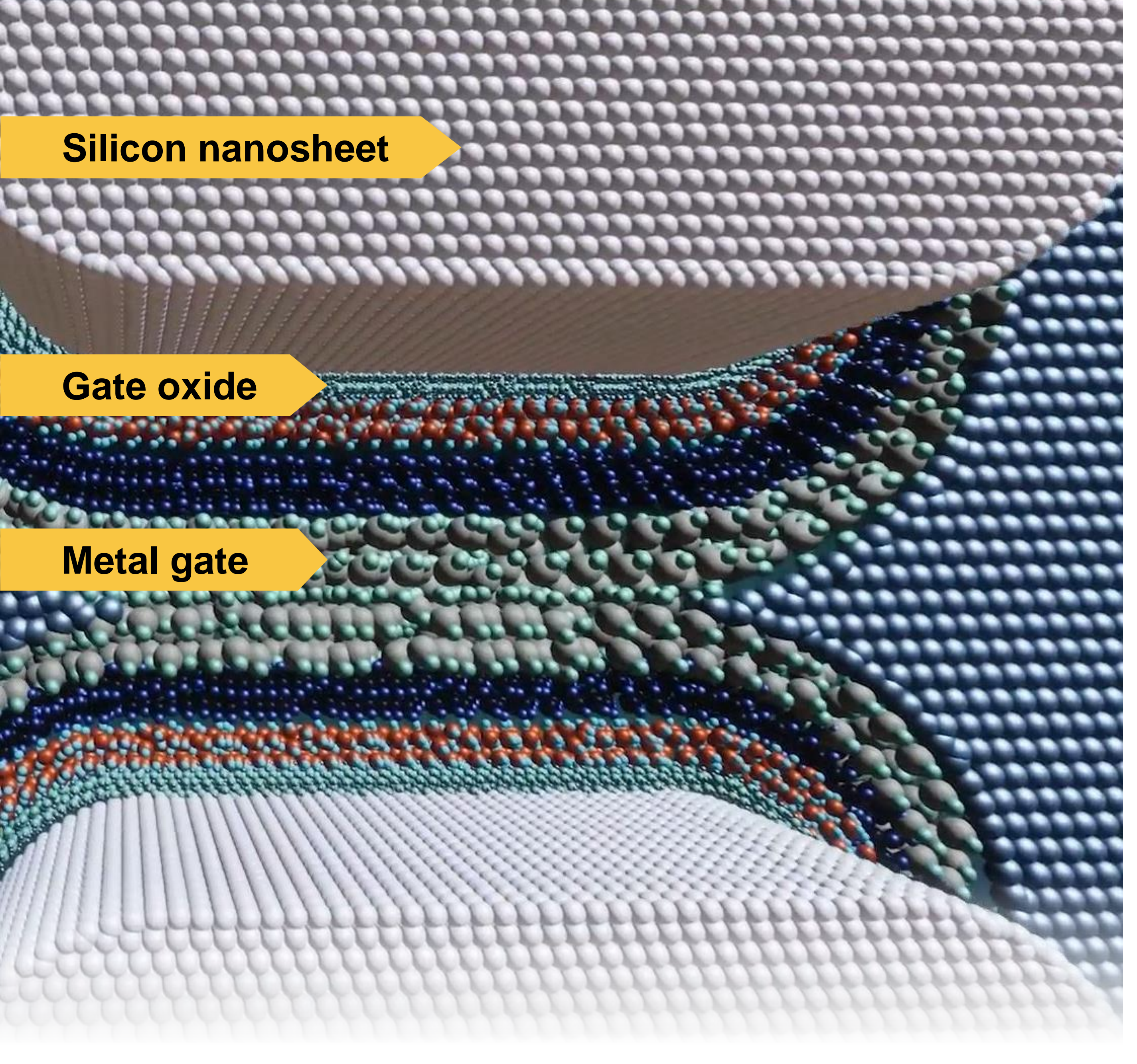
FinFET



GAA
33% improvement
in energy efficiency

Source: TSMC
GAA: gate-all-around
FET: field-effect-transistor

New materials, selective deposition and removal, and process step interactions



VIEW OF
PROCESS COMPLEXITY
(GAA Transistor)

In just ~10nm between nanosheets:

- >5 distinct materials
- 1–2nm per layer of material

Engineered with angstrom-level precision across more than **ten trillion transistors** at a time

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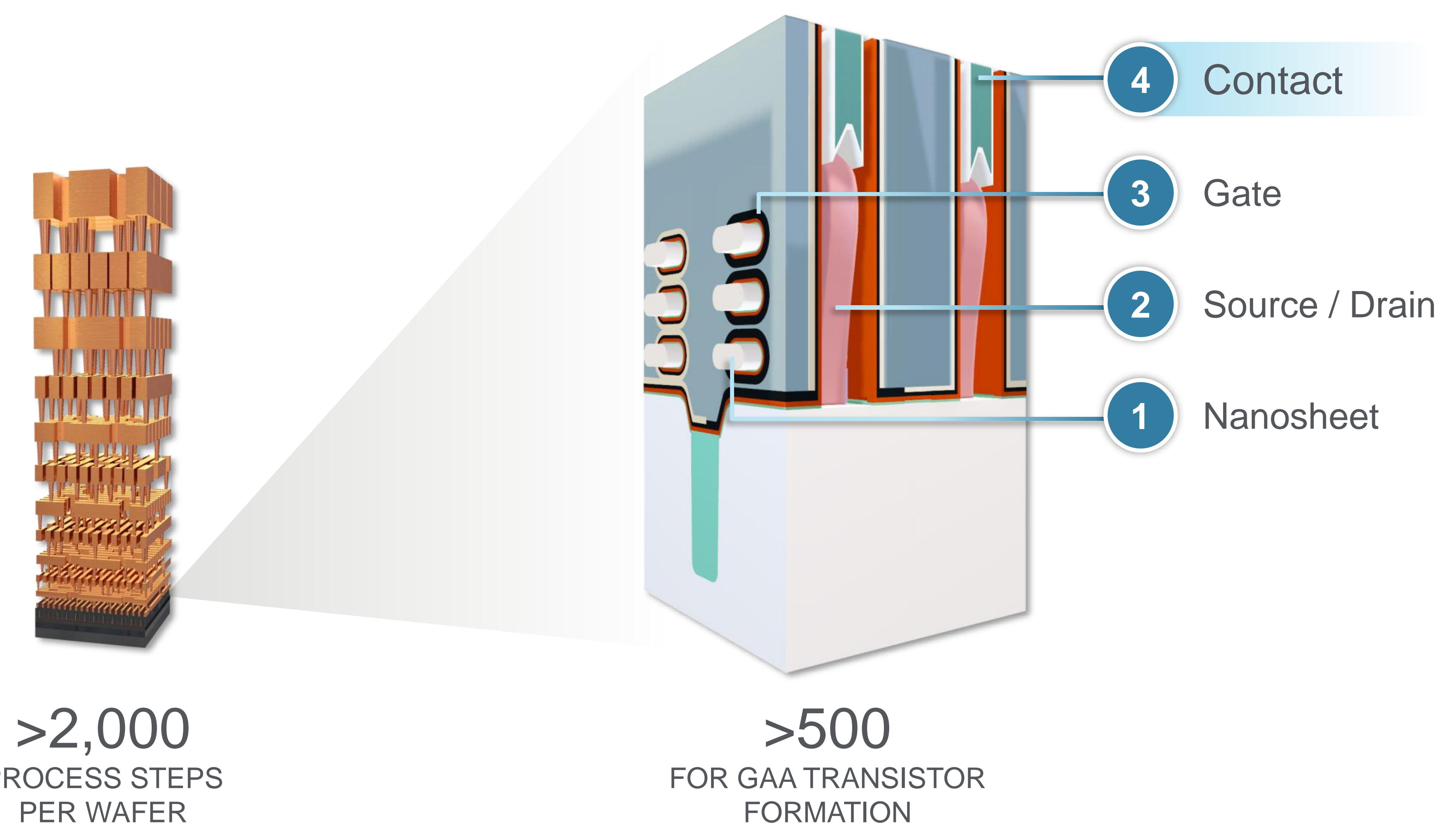
GAA Transistor: 4 Major Modules



>2,000
PROCESS STEPS PER WAFER

>500
FOR GAA TRANSISTOR FORMATION

GAA: gate-all-around

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GAA Contact Engineering

metal

dielectric

metal

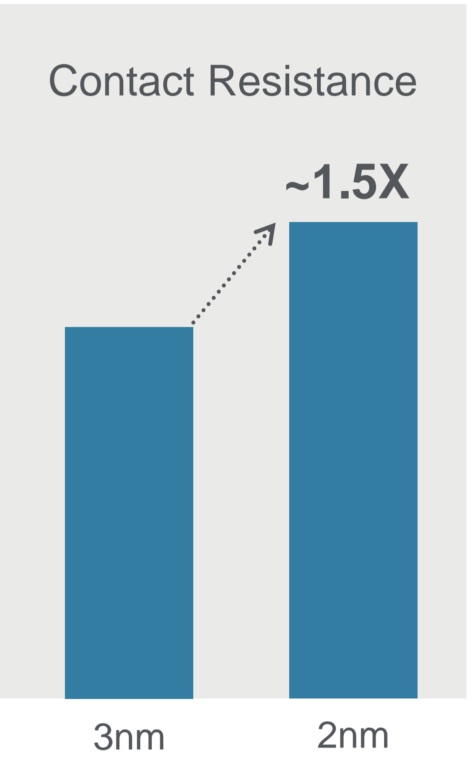
spacer

metal gate stack

Si nanosheet channel

source

drain



Shrinking the contact area increases contact resistance

GAA: gate-all-around

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GAA Transistor Contact | Example of Increasing Process Complexity

Co-optimized etch and deposition processes

Applied Integrated Materials Solution

Applied Integrated Materials Solution

- Clean
- **Deposition hardmask**
- **Deposition patterning film**
- Track photoresist
- Lithography trench pattern
- Lithography contact pattern
- **Etch patterning film open**
- **Etch hardmask open**
- Etch inter-layer dielectric oxide
- Ash/etch patterning films
- ALD liner deposition
- **Etch source-drain cavity shaping**
- **Epitaxial contact deposition**
- Silicide deposition and anneal
- **Metal cap deposition**
- **Treatment**
- **Metal fill**
- CMP metal overburden removal

MODULE ~20 STEPS

2 co-optimized processes, 2 integrated solutions

metal
dielectric
metal
spacer
metal gate stack
Si nanosheet channel
source
drain

Note: General process flow

High complexity requires connecting broad set of capabilities

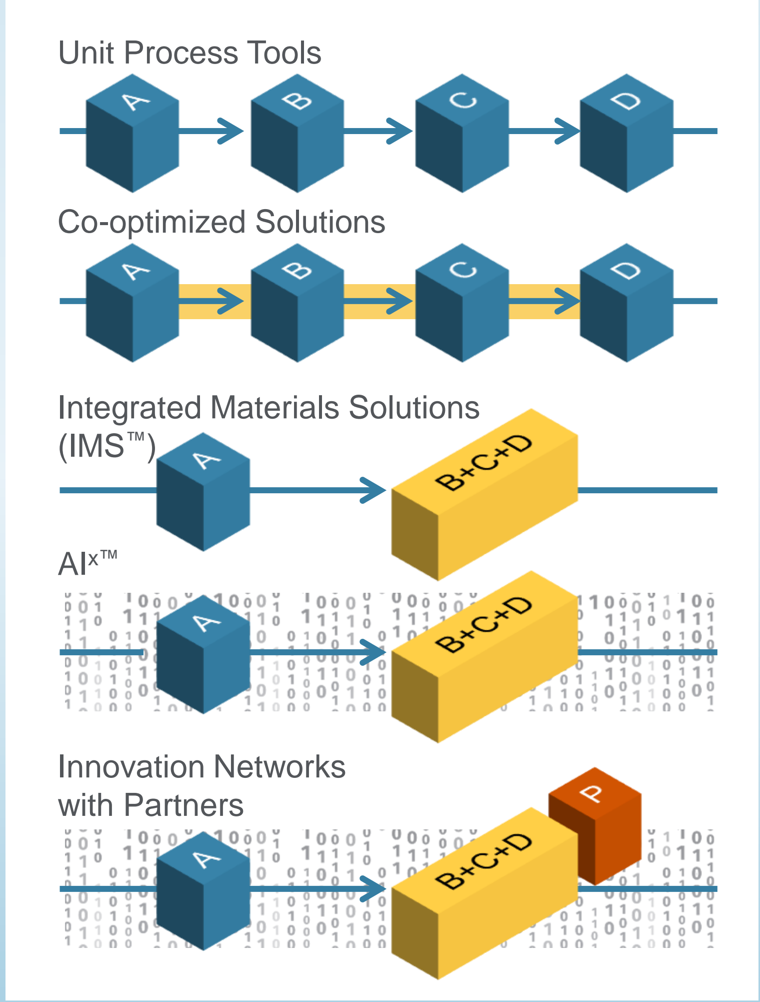
GAA: gate-all-around
ALD: atomic layer deposition
CMP: chemical mechanical planarization

Applied's Unique Connected Materials Engineering Portfolio

BROADEST CAPABILITIES

	Applied	Competitors				
ALD	✓	✓			✓	✓
Cleans					✓	✓
CMP	✓					
CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace						✓
Implant	✓					
Lithography			✓			
PDC	✓		✓	✓		
PVD	✓			✓		
Thermal	✓					✓
Track						✓

UNIQUE COMBINATIONS



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GAA Contact | Integration Improves Resistance, Speed, Power

Co-optimized etch and deposition processes

- Clean
- **Deposition hardmask**
- **Deposition patterning film**
- Track photoresist
- Lithography trench pattern
- Lithography contact pattern
- **Etch patterning film open**
- **Etch hardmask open**
- Etch inter-layer dielectric oxide
- Ash/etch patterning films
- ALD liner deposition
- **Etch source-drain cavity shaping**
- **Epitaxial contact deposition**
- Silicide deposition and anneal
- **Metal cap deposition**
- **Treatment**
- **Metal fill**
- CMP metal overburden removal

Applied Integrated Materials Solution (Etch source-drain cavity shaping; Epitaxial contact deposition)

Applied Integrated Materials Solution (Metal cap deposition; Treatment; Metal fill)

Applied Integrated Materials Solution

Contact Resistance
Silicon Interface

50%

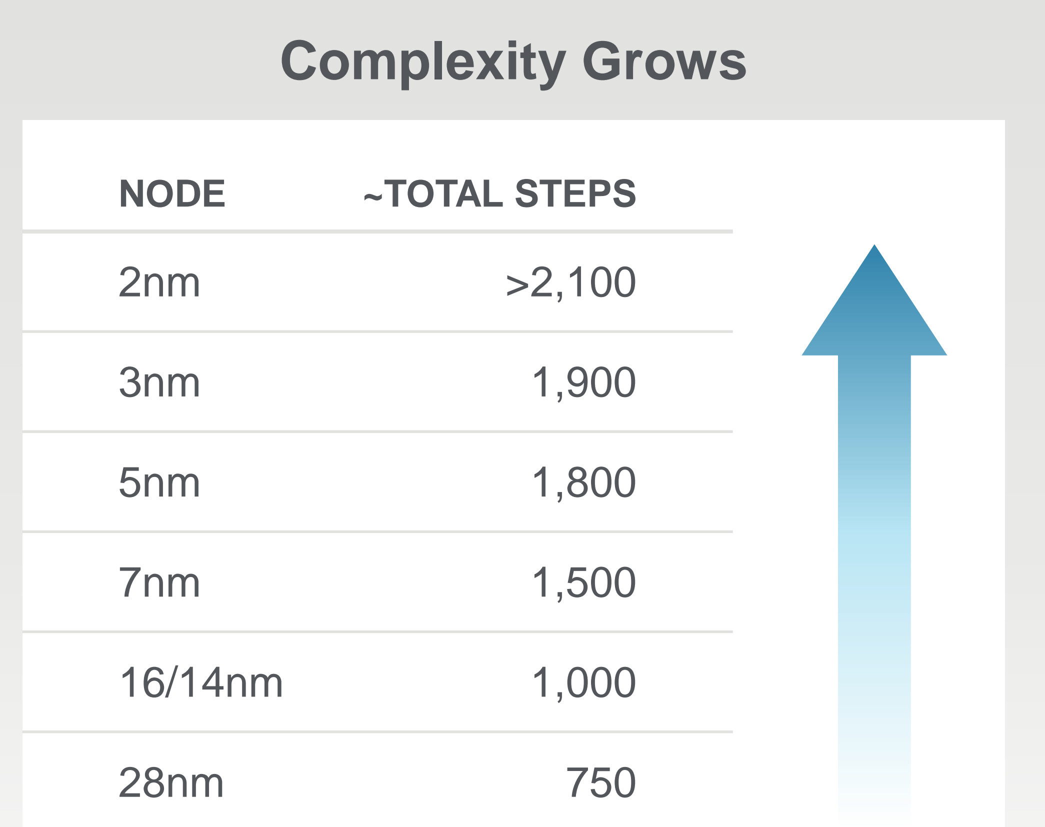
Non-Integrated | Integrated

Note: General process flow

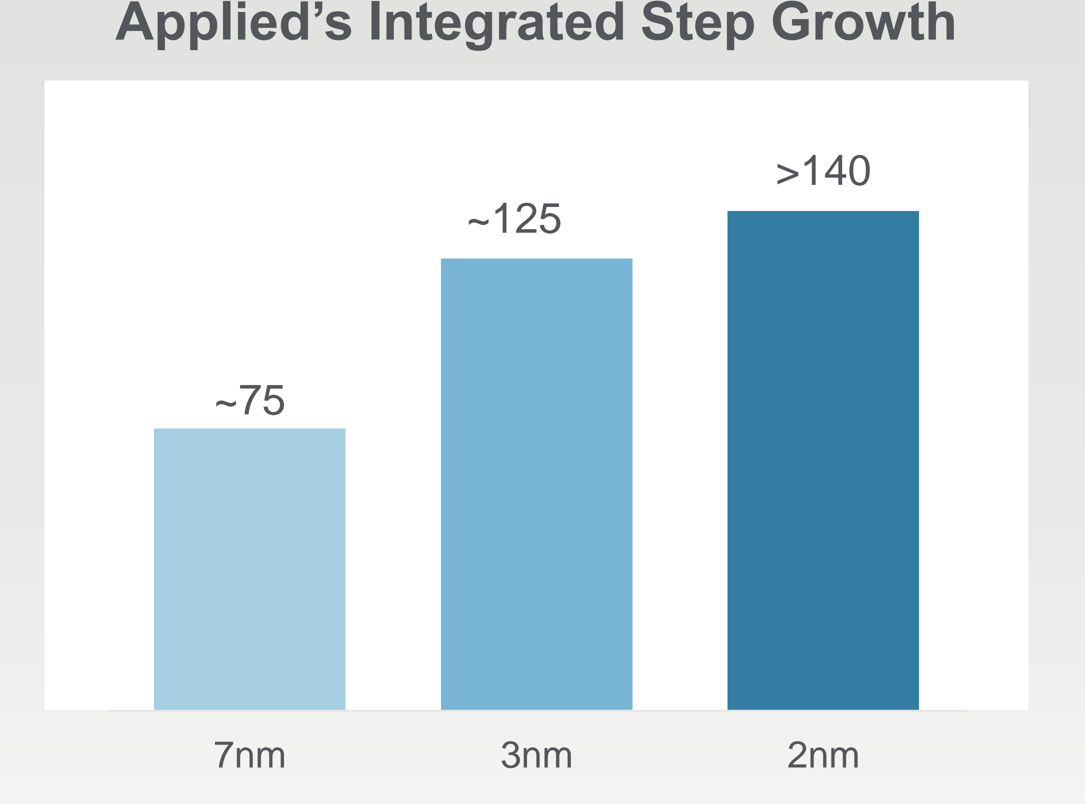
Connecting broad set of products improves performance

GAA: gate-all-around
ALD: atomic layer deposition
CMP: chemical mechanical planarization

Demand for Integrated Solutions Growing with Device Complexity



NODE	~TOTAL STEPS
2nm	>2,100
3nm	1,900
5nm	1,800
7nm	1,500
16/14nm	1,000
28nm	750



APPLIED MATERIALS®

Applied's Playbook for Accelerating Connectivity

1

Connect our unique portfolio of materials engineering products

2

Connect Applied's innovators to accelerate invention of novel solutions: new organization structure

3

Connect with customers and partners, earlier and deeper, to co-innovate the industry roadmap

2013

2018

2023

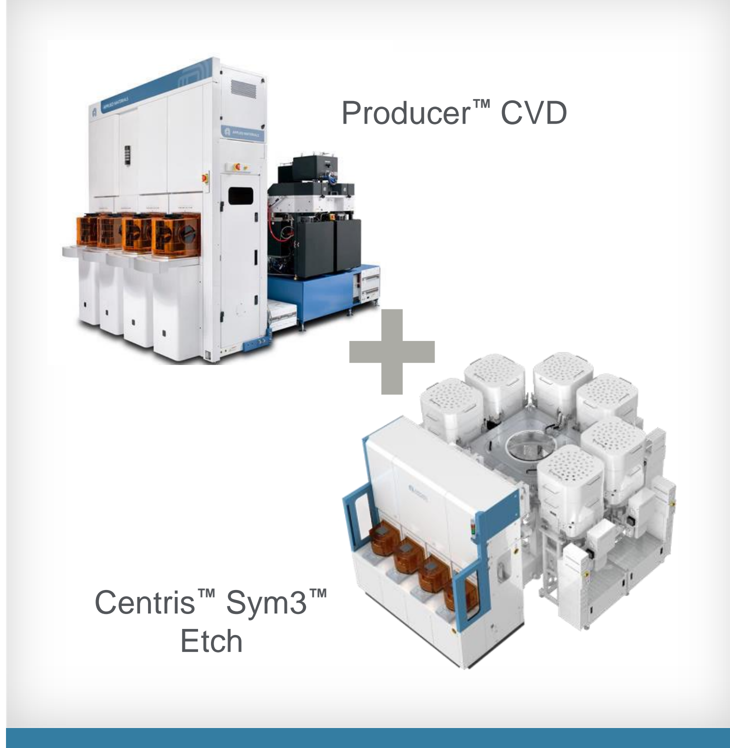
APPLIED MATERIALS®

Connecting Applied's Unique Materials Engineering Portfolio

Endura™ PVD

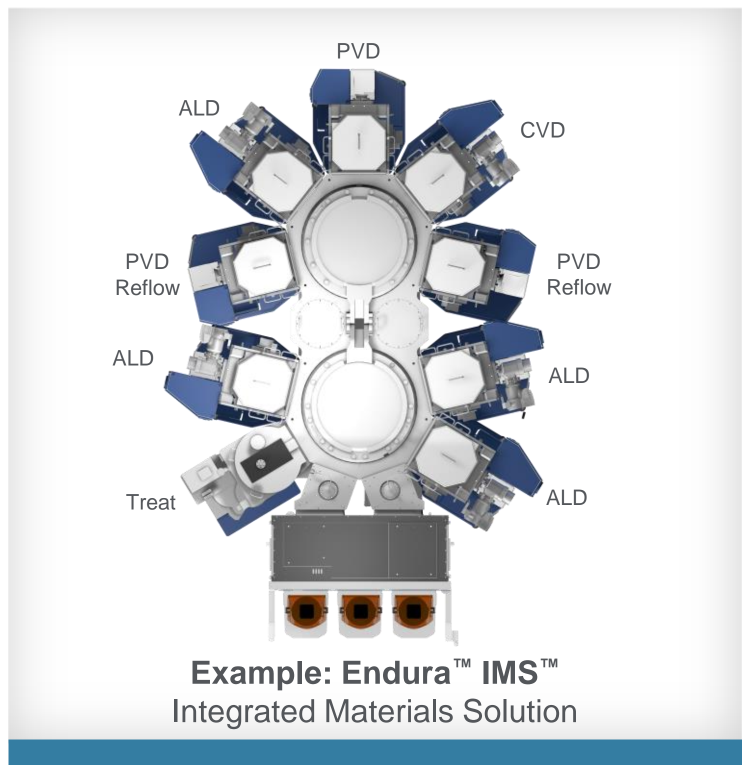
Unit Processes

One technology
in one system



Co-optimized Processes

Two or more co-optimized
technologies in adjacent systems



Example: Endura™ IMS™
Integrated Materials Solution

Integrated Processes

Two or more co-optimized
technologies in one system

APPLIED MATERIALS

2018
2

Connecting Applied's Innovators to Invent Novel Solutions

NEW ORGANIZATIONS

- Integrated Materials Solutions (IMS™)
- ICAPS*
- Heterogenous Integration (HI)
- Actionable Insight Accelerator (AIx™)
- Systems-to-Materials

ACCELERATORS

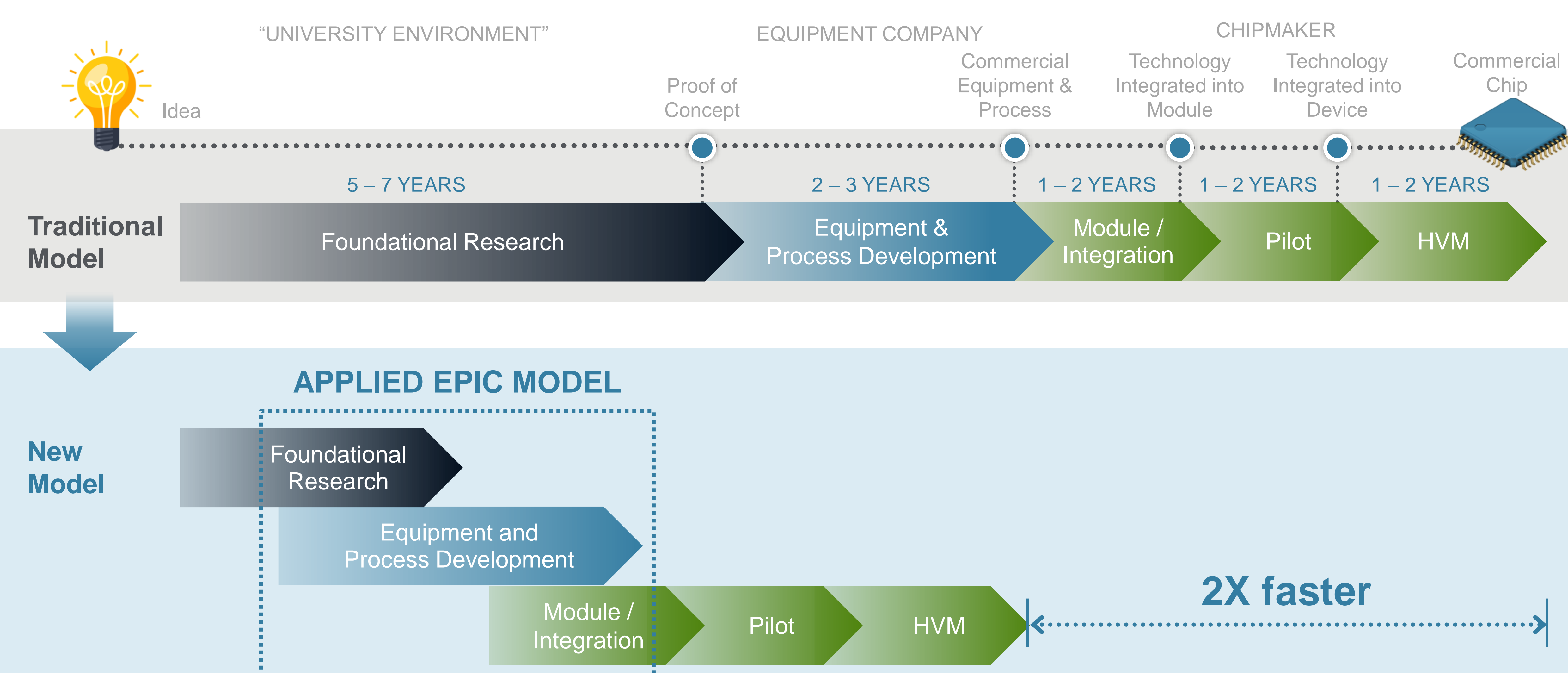
Maydan Technology Center

Materials Engineering Technology Accelerator

Advanced Packaging Development Center

*Internet of Things, Communications, Automotive, Power and Sensors

Connecting Partners to Accelerate the Industry Roadmap



APPLIED MATERIALS

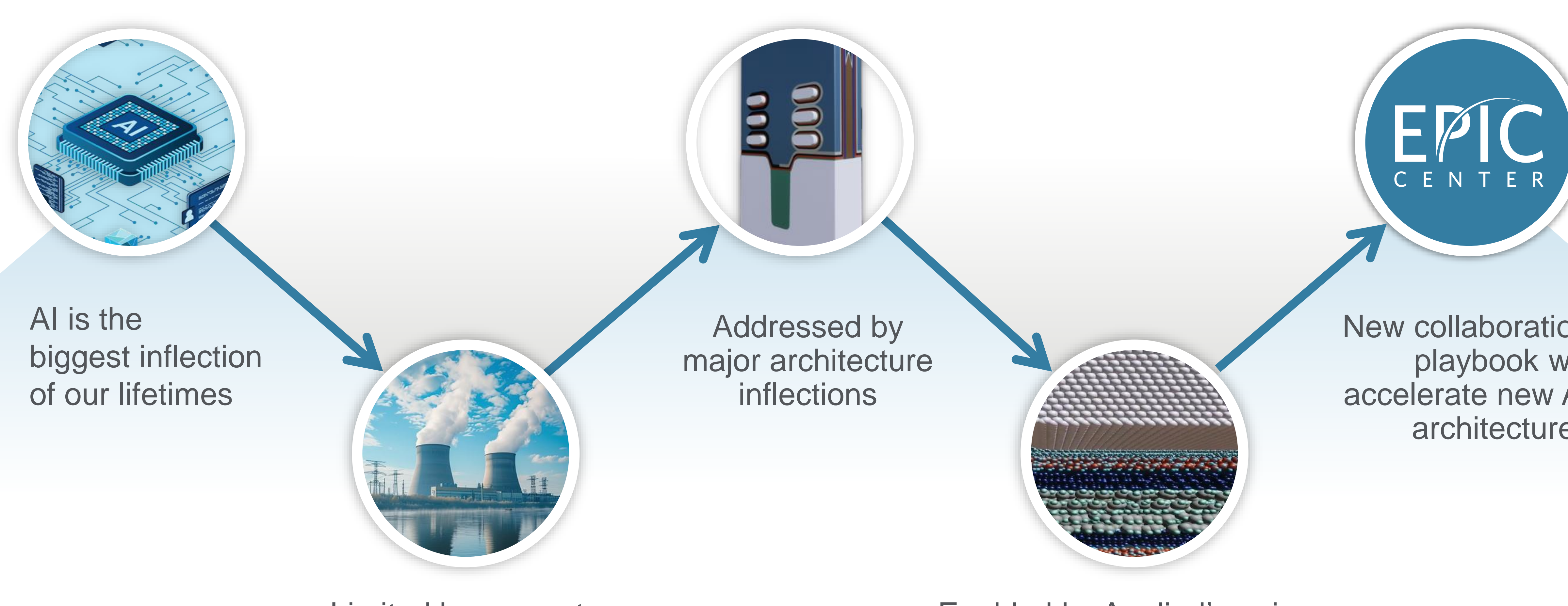
"Modern semiconductor technology cannot be successfully developed by a single company. Therefore, Samsung Electronics is conducting various **collaborations with Applied Materials across all areas of future technology** through process development to develop next-generation **memory** semiconductors, including **HBM**, artificial intelligence and cloud computing-oriented **logic** products. We will continue to shape the semiconductor industry ecosystem and through constant innovation, overcome the technological limitations to **prepare for the AI era with you.**"

JAIHYUK SONG, PH.D.

Corporate President, Device Solutions
CTO, Samsung Electronics

APPLIED MATERIALS

Fueling the Race for AI Leadership



AI is the biggest inflection of our lifetimes

Limited by compute energy-efficiency

Addressed by major architecture inflections

Enabled by Applied's unique and connected materials engineering portfolio

New collaboration playbook will accelerate new AI architectures

APPLIED MATERIALS®

AGENDA

7:35 Prabu Raja, Ph.D.
Race for AI Leadership
Fueled by Materials Engineering

7:55 Mark Fuselier, AMD
Power and Performance in the AI Era

8:10 Mukund Srinivasan, Ph.D.
Enabling the AI Device Inflections

8:20 Device Inflection Expert Panel

» Mehul Naik, Ph.D. — Transistors and Wiring
» Sony Varghese, Ph.D. — DRAM
» Jinho An, Ph.D. — High-Bandwidth Memory
» Sarah Wozny, Ph.D. — Heterogeneous Integration

8:50 Prabu Raja, Ph.D.
Growing our Opportunity and Share

Power and Performance in the AI Era

Mark Fuselier
Senior Vice President, Technology and Product Engineering
AMD

JULY 9, 2024

Enabling the Device Inflections

Mukund Srinivasan, Ph.D.
Vice President and General Manager, Semiconductor Products Group

JULY 9, 2024

CALL TO ACTION

1. Logic: More transistors operating at lower power
2. Memory: Higher capacity and bandwidth, lower latency
3. Packaging: Tightly integrated logic, memory and I/O to increase energy-efficient performance

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8:50 Prabu Raja, Ph.D.
Growing our Opportunity and Share

Driving Energy-Efficient Performance: Improves 3X Every 2 Years

Projected

100
1
0.01
0.0001
0.000001

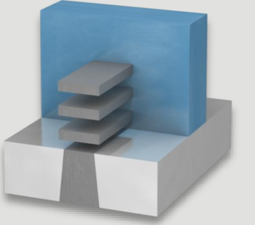
EEP (1/(fJ·psec))

2005 2010 2015 2020 2025 2030 2035 2040

Year

Energy-Efficient Performance Drivers Include:

1. New transistors and materials



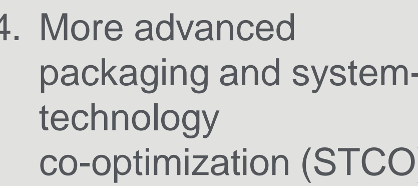
New Transistor
GAA

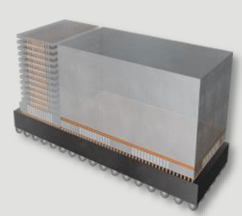
2. EUV lithography plus design-technology co-optimization (DTCO)

DTCO
Backside Power

3. Circuit and architecture innovations

4. More advanced packaging and system-technology co-optimization (STCO)





STCO
Heterogeneous Integration

Energy-efficient performance (EEP) = Throughput/Watt × Throughput, in units of 1/(fJ·psec). Data are based on server GPU data.

Source: Mark Liu and H.-S. Philip Wong, IEEE Spectrum, March 28, 2024. https://spectrum.ieee.org/trillion-transistor-gpu

GAA: gate-all-around

DTCO: Another Way to Increase Transistors per Chip

Intrinsic Scaling (Litho)

N

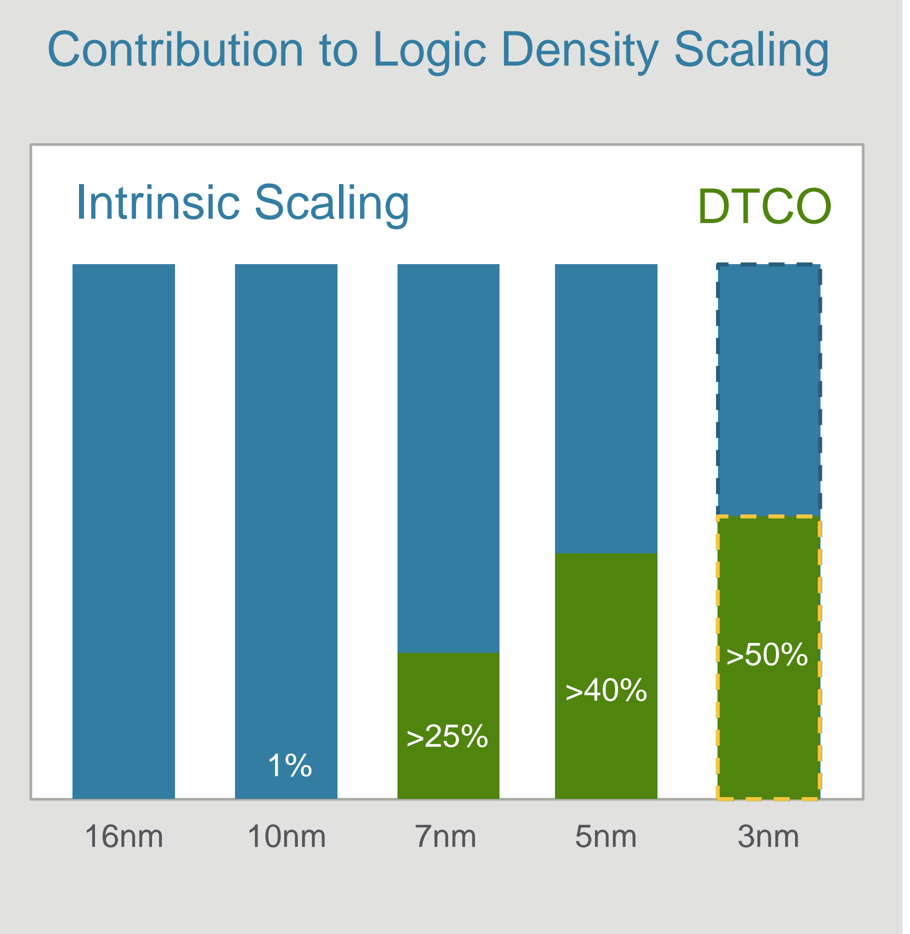
N+1

DTCO

N

N+1

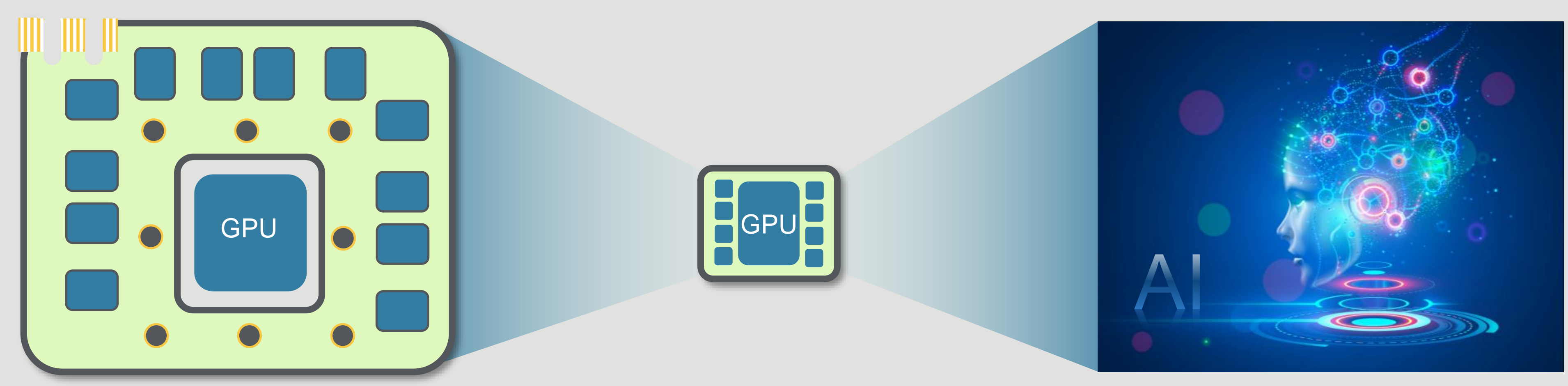
Source: M. Liu/TSMC, ISSCC 2021



DTCO: Design Technology Co-Optimization

DTCO is enabled by materials engineering

STCO: Improves System Energy Efficiency by Orders of Magnitude



Packaging Interconnect Scaling	Bump	Microbumps	TSV	Hybrid Bonding
I/O Density (I/O per mm^2)	10^2	10^3	10^4	10^4 to 10^6
Energy (picoJ per bit)	1.5	0.5	0.1	0.05

STCO is enabled by materials engineering

STCO: system technology co-optimization
GPU: graphical processing unit
HBM: high-bandwidth memory
TSV: through-silicon via
I/O: input/output

APPLIED MATERIALS

Co-Innovating with Our Partners: The Global EPIC Platform

Maydan Technology Center, Sunnyvale CA

META Center, Albany NY

Advanced Packaging Dev. Center, Singapore

EPIC Center™ (Planned), Sunnyvale CA

Deploying our broad, deep and connected portfolio of materials engineering solutions to support **high-velocity innovation and commercialization** of next-generation technologies

Anticipating inflections and delivering solutions critical to competitive advantage in fast-growing markets

Changing the industry's innovation model to accelerate mutual success rates and increase return on investment

META: Materials Engineering Technology Accelerator; EPIC: Equipment and Process Innovation and Commercialization

"AI workloads demand massive compute memory capacity and bandwidth. To meet these demands, Micron is adopting novel manufacturing technologies for new DRAM transistor architectures and advanced packaging for higher bandwidth. **With Applied Materials and its partners, we can rapidly access an expansive and connected toolkit of solutions to bring our revolutionary designs to life."**

NAGA CHANDRASEKARAN, PH.D.

Senior Vice President, Technology Development
Micron Technology, Inc.

Device Inflection Expert Panel

Mehul Naik, Ph.D.

Vice President of Technology, Semiconductor Products Group

Sony Varghese, Ph.D.

Sr Director of Technical Marketing, Semiconductor Products Group

Jinho An, Ph.D.

Account Technologist Director, Semiconductor Products Group

Sarah Wozny, Ph.D.

Director, Semiconductor Products Group

Transistors and Wiring

Mehul Naik, Ph.D.
Vice President of Technology, Semiconductor Products Group

JULY 9, 2024

The Transistor Roadmap

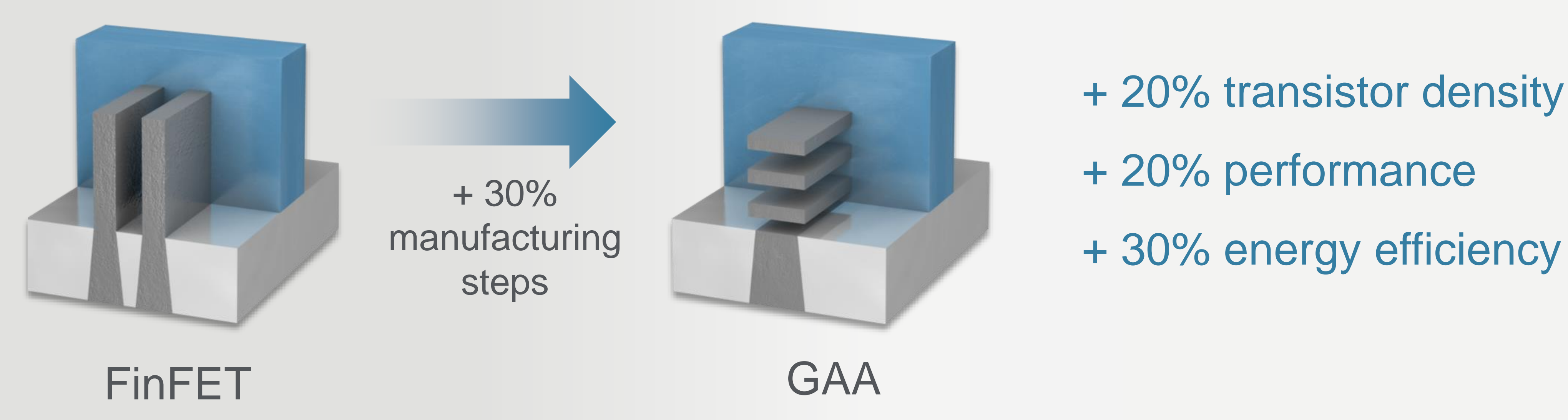
Planar

FinFET

GAA

FET: field effect transistor; GAA: gate-all-around

Building the Gate-all-around Transistor



Source: Jaehun Jeong, Samsung, 2023 VLSI
FET: field effect transistor; GAA: gate-all-around

Applied offers more than 10 technologies to build gate-all-around transistors

Gate-All-Around and Beyond

N
P
N
P

GAA

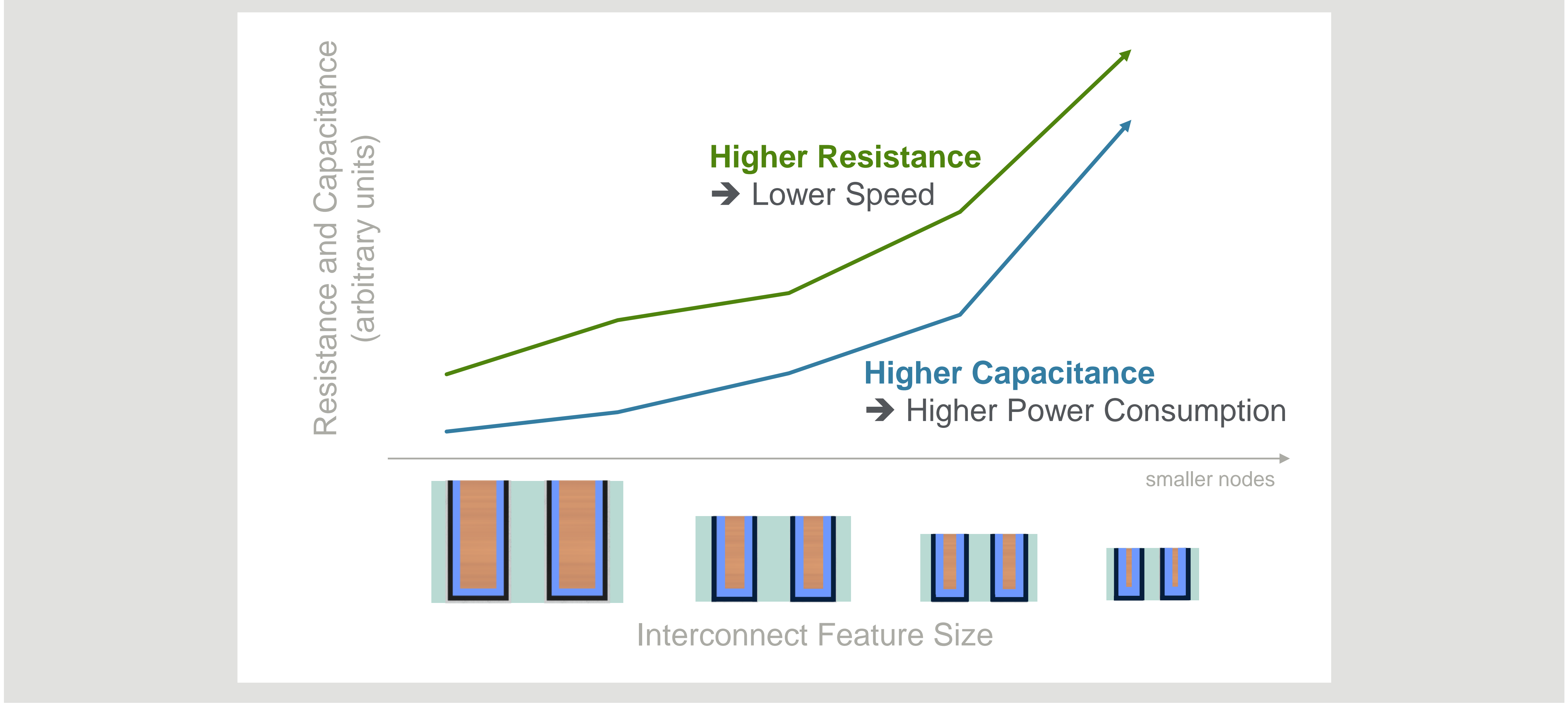
GAA with
Backside Power

GAA with Isolation

CFET

GAA: gate-all-around
CFET: complementary field effect transistor

Shrinking Interconnects Degrade Power and Speed



Note: General R and C Trends

APPLIED MATERIALS

Applied's Leadership in Interconnect Manufacturing

Source: TechInsights

Copper Line

Via

Line

Dielectric (CVD)
Develop and deposit specialized materials

Barrier (ALD)
Prevent copper migration

Cobalt Liner (CVD)
Promote uniform copper fill

Copper Reflow (PVD)
Void-free line and via fill

Planarization (CMP)
Remove excess copper to form low-resistance, reliable wire

CVD: chemical vapor deposition; ALD: atomic layer deposition; PVD: physical vapor deposition; CMP: chemical mechanical planarization

Wiring Innovations for the AI Era

Press Release

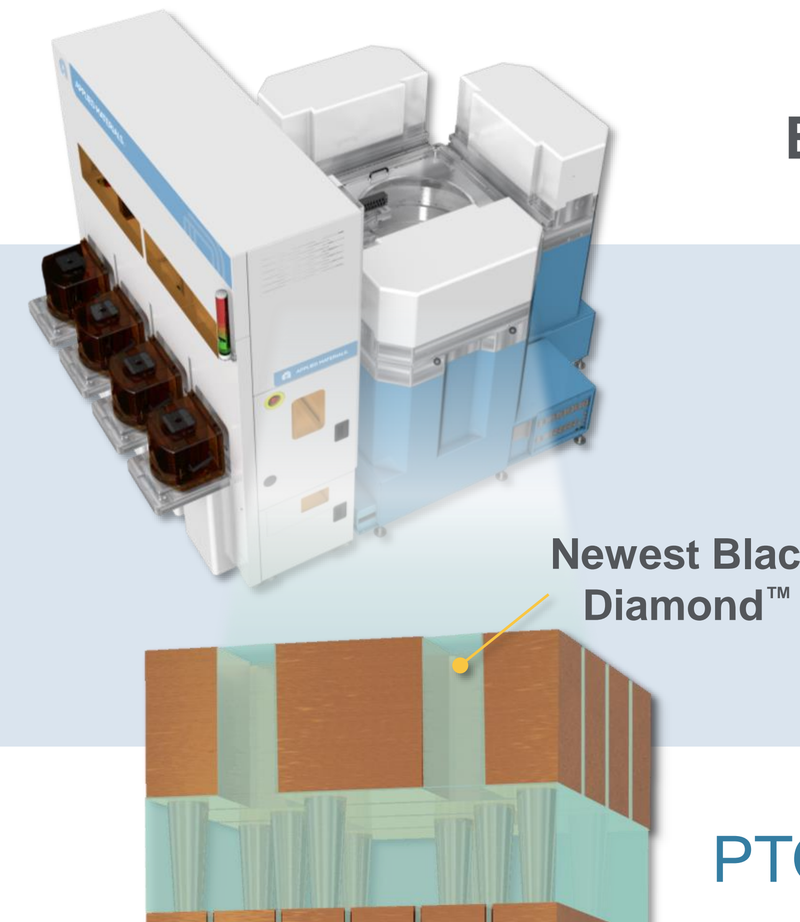
NEWS RELEASE

Applied Materials Unveils Chip Wiring Innovations for More Energy-Efficient Computing

- *Industry's first use of ruthenium in high-volume production enables copper chip wiring to be scaled to the 2nm node and beyond and reduces resistance by as much as 25%*
- *New enhanced low-k dielectric material reduces chip capacitance and strengthens logic and DRAM chips for 3D stacking*

SANTA CLARA, Calif., July 8, 2024 – Applied Materials, Inc. today introduced materials engineering innovations designed to increase the performance-per-watt of computer systems by enabling copper wiring to scale to the 2nm

Newest Black Diamond™ Low-k Dielectric Film



Enabling interconnect scaling for 2nm and beyond

- ✓ Lower capacitance for faster signals and lower power
- ✓ Increased mechanical strength for 3D die stacking
- ✓ Designed for all frontside and backside wiring

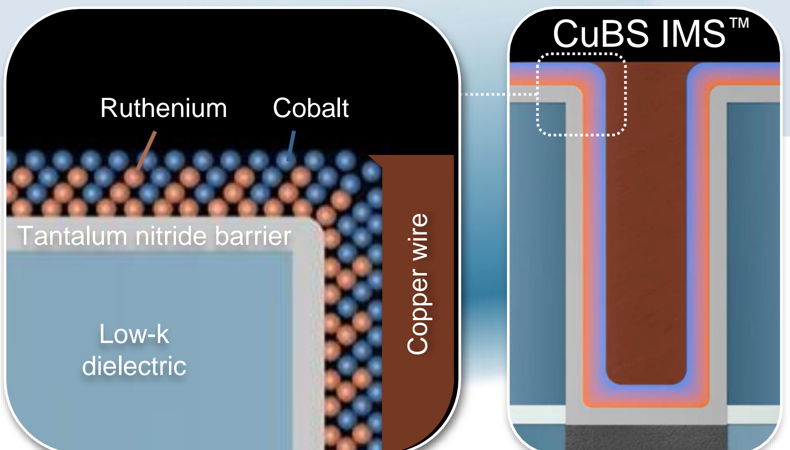
PTOR at multiple leading-edge logic and DRAM chipmakers

PTOR: production tool of record

Introducing Endura™ Copper Barrier Seed IMS™ with Volta™ Ru CVD

Enabling interconnect scaling for 2nm and beyond

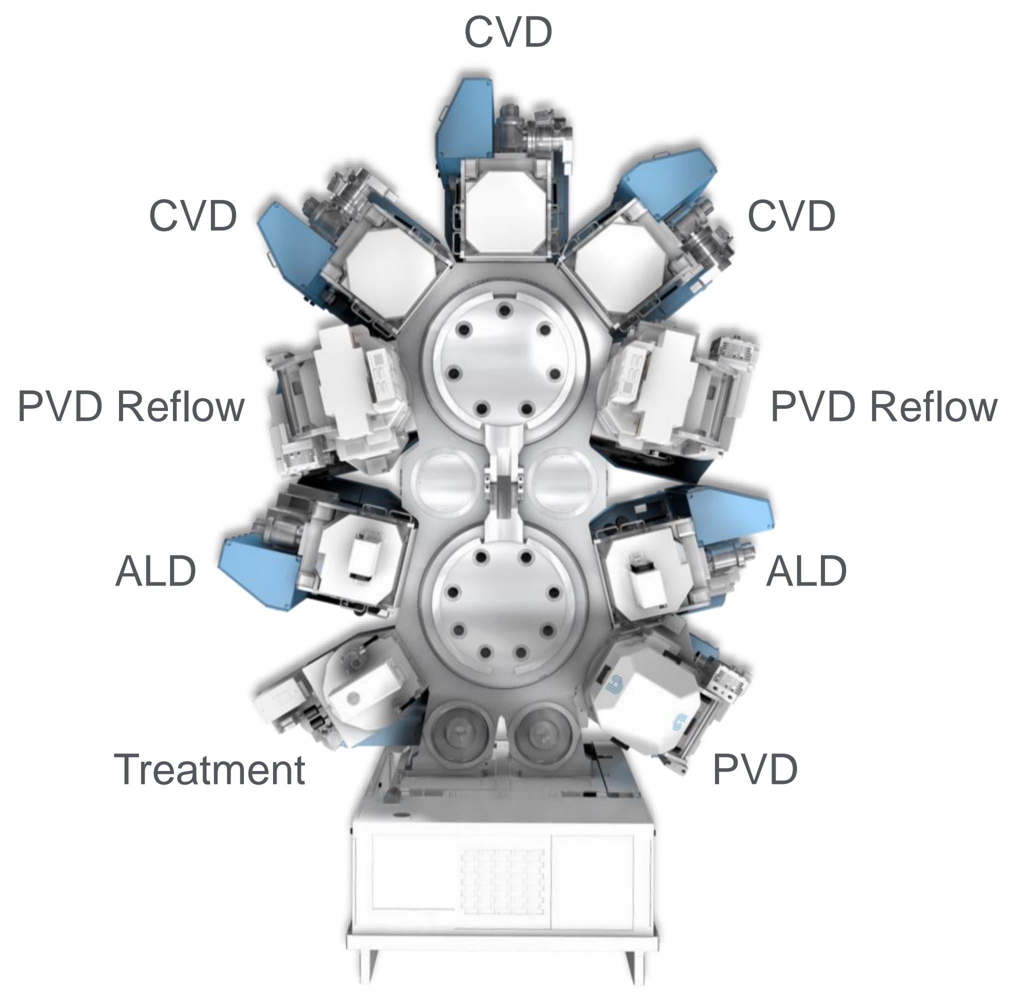
- ✓ Binary system of ruthenium and cobalt enables void-free copper reflow to maximize reliability and increase yield
- ✓ Thin binary liner maximizes copper volume
- ✓ 25% lower electrical resistance significantly reduces chip power consumption
- ✓ Enhances the most critical metal layers



DTOR at all leading-edge logic chipmakers

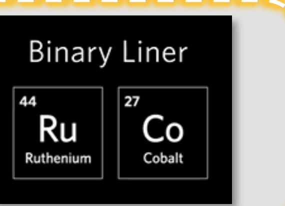
CuBS: copper barrier seed
IMS: integrated materials solution
DTOR: development tool of record

Integrated Materials Solution for 2nm Node and Beyond



Endura™ CuBS IMS™ with Volta™ Ru CVD

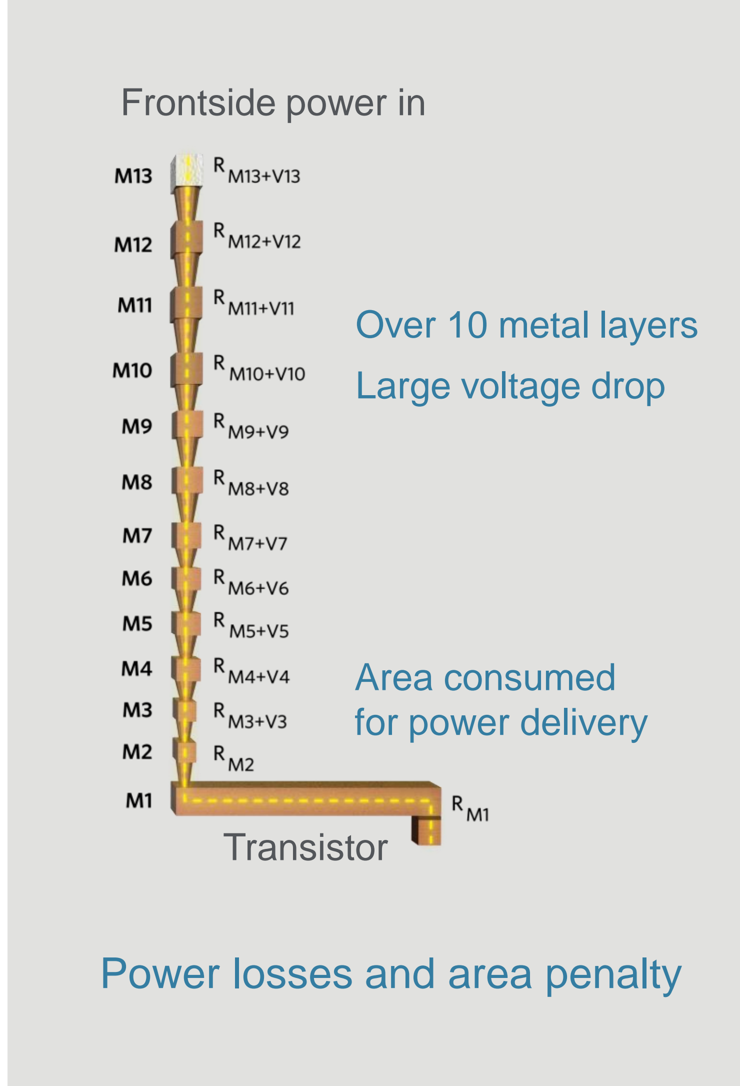
1. Surface Preparation
2. Barrier Deposition
3. Material Modification
4. Ruthenium Deposition
5. Cobalt Deposition
6. Copper Reflow

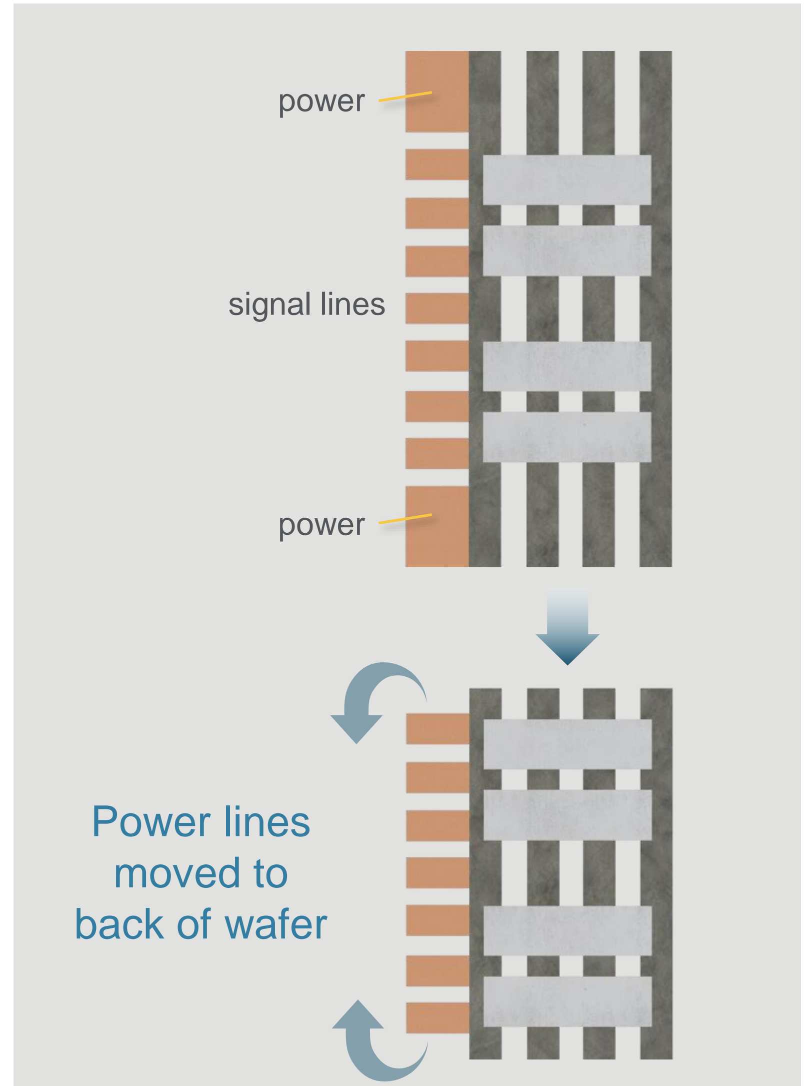


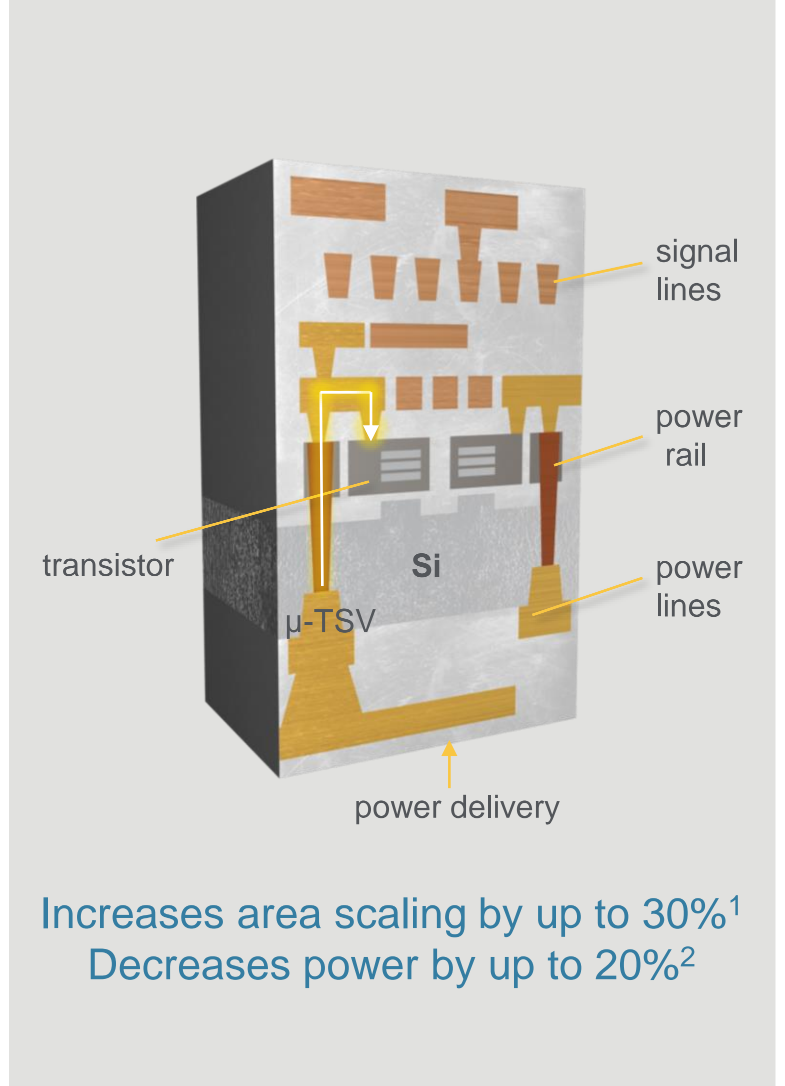
ALD: atomic layer deposition; CVD: chemical vapor deposition; PVD: physical vapor deposition, CuBS: copper barrier seed, IMS: integrated materials solution

APPLIED MATERIALS

Backside Power Delivery







Source: 1 J. Ryckaert et al., 2019 EDTM, 2 TSMC 2024 Symposium; μ-TSV: micro-through-silicon-via

Multiple Approaches with Scaling vs. Complexity Trade-offs

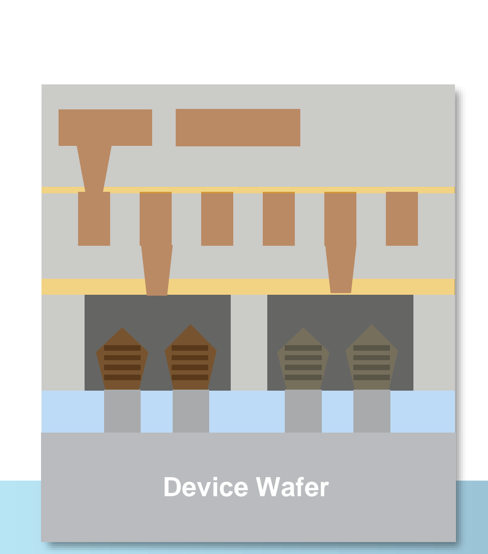
	Buried Power Rail	Power Via	Direct Backside Contact
	buried power rail n-TSV power delivery	power via power delivery	backside contact power delivery
Area Scaling	Good	Better	Best
Process Complexity	Low	Medium	High

Source: Adapted from Song et al. (IEDM, 2021) with subsequent analysis by Applied Materials

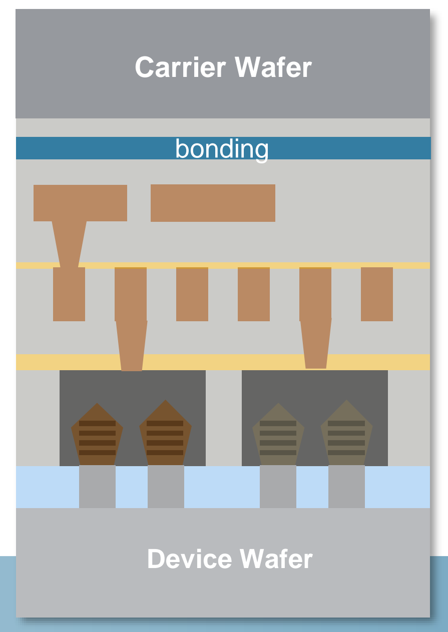
Source: Adapted from public company disclosures (2021) with subsequent analysis by Applied Materials

Source: Adapted from Song et al. (IEDM, 2021) with subsequent analysis by Applied Materials

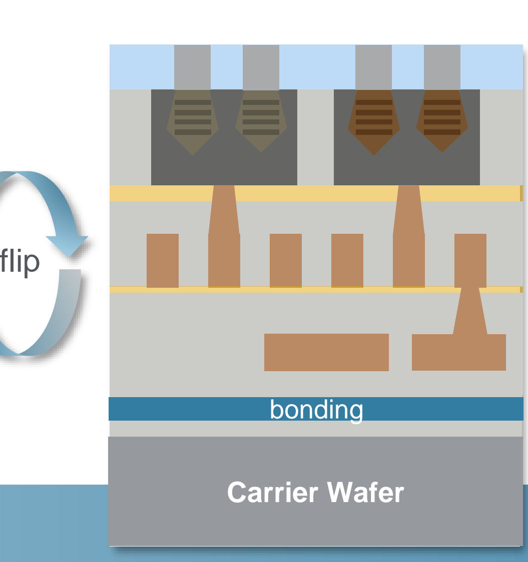
Simplified Direct Backside Contact (DBC) Process Flow



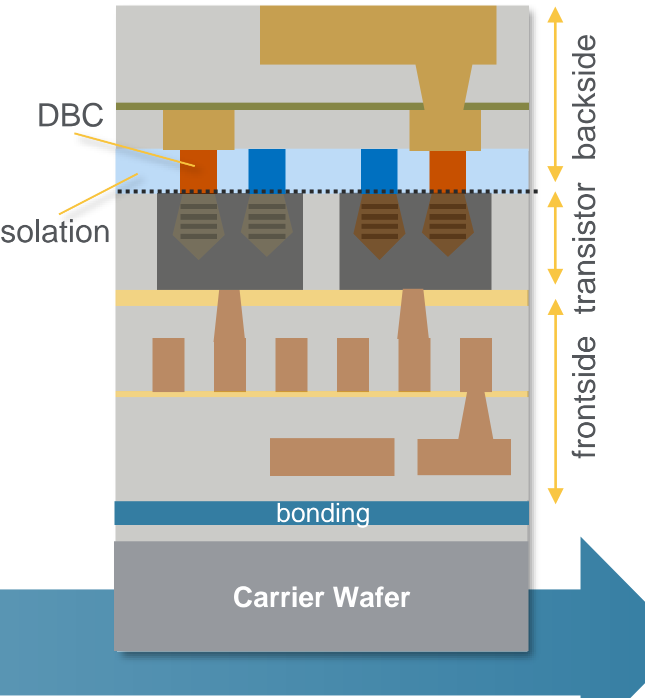
- transistors
- contact / MOL
- interconnect



- fusion bond to carrier wafer



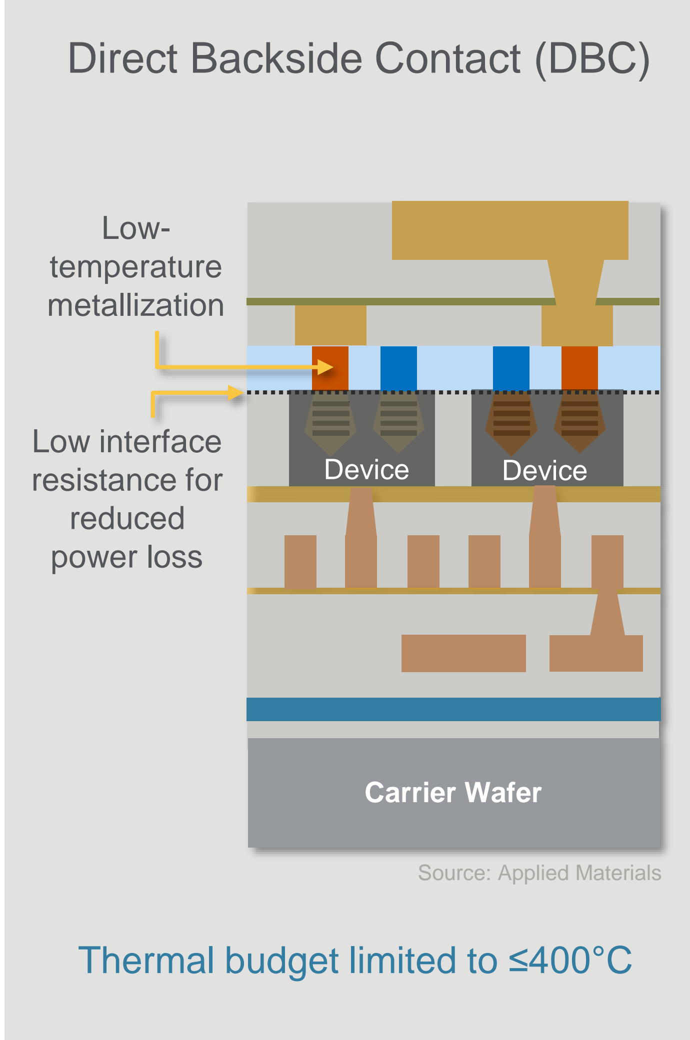
- flip wafer
- extreme wafer thinning



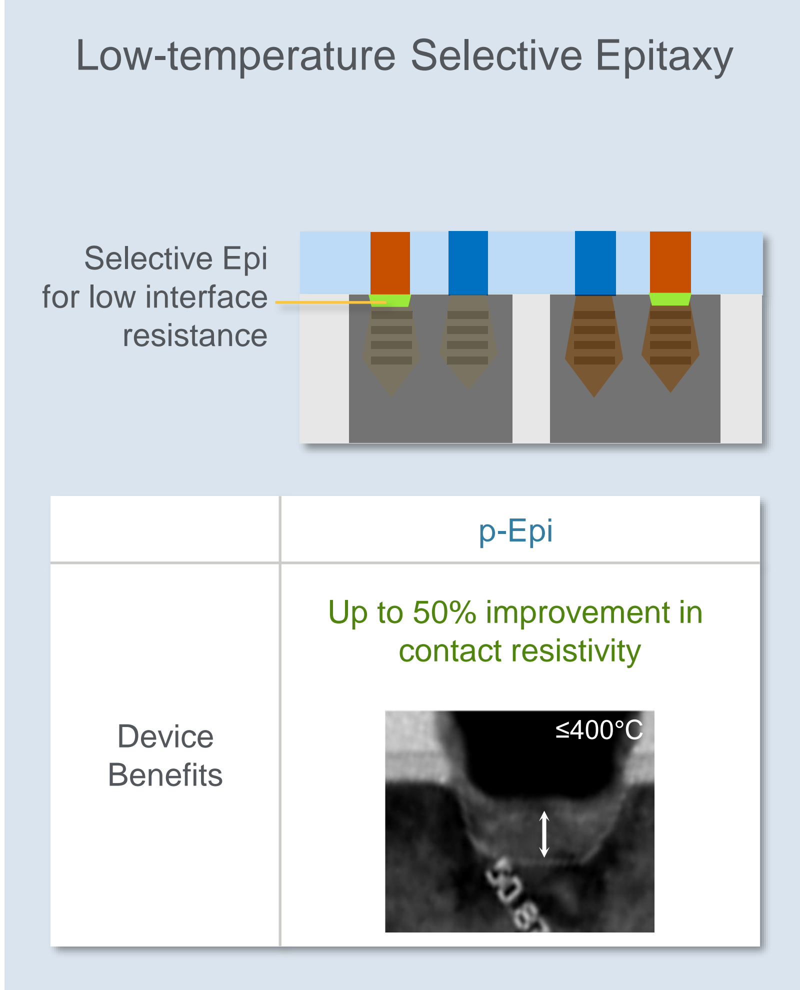
- backside isolation
- DBC lithography
- low-temperature DBC formation
- backside interconnect

MOL: middle-of-line

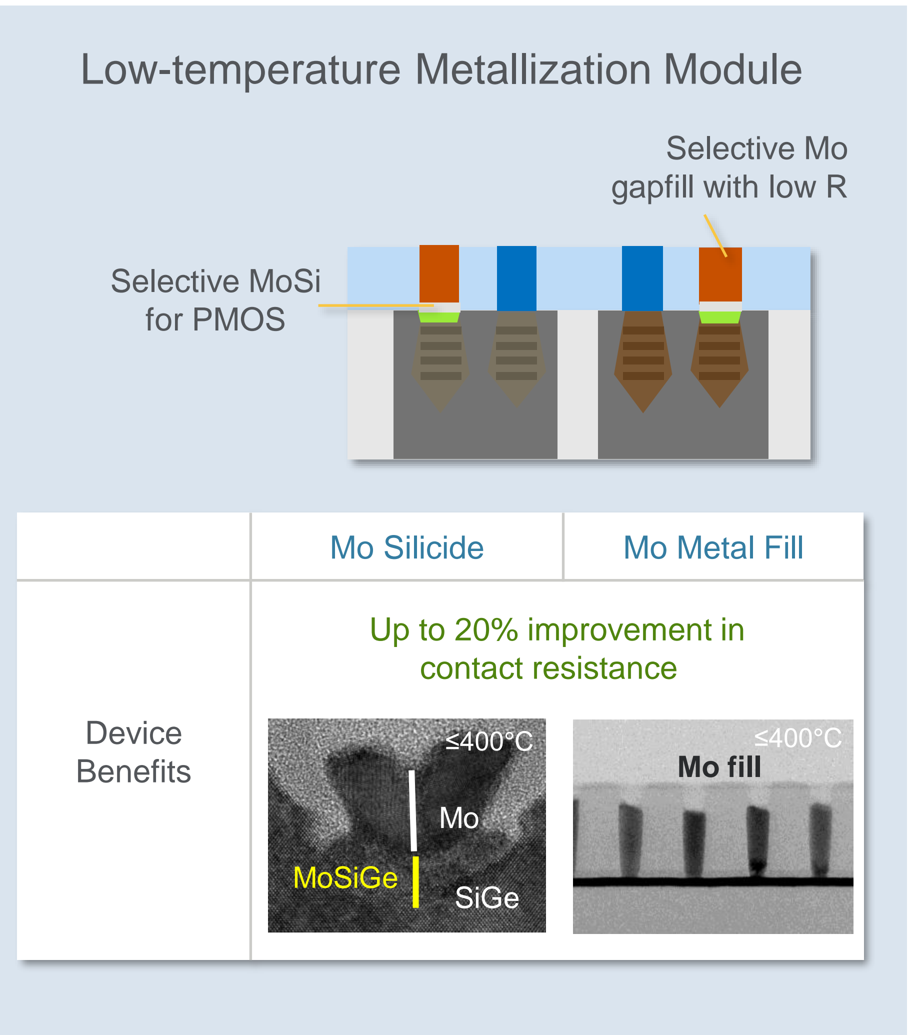
DBC Technology Challenges: Low-temperature Backside Contact



Source: Adapted from Song et al. (IEDM 2021)



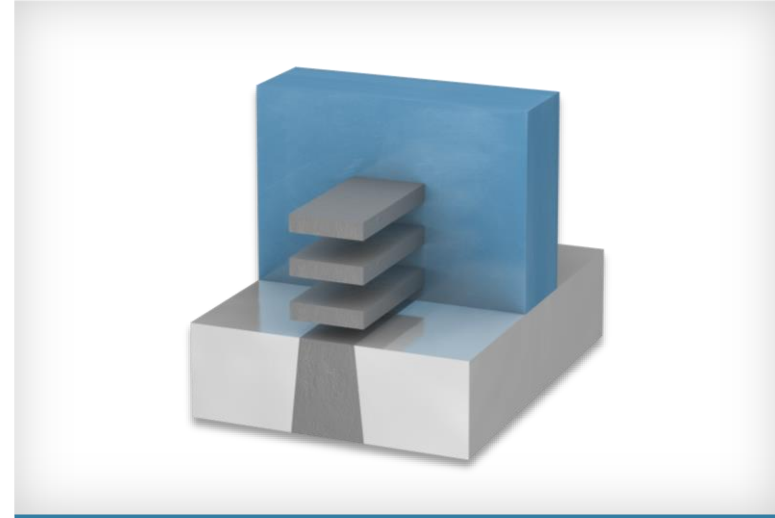
Source: N. Briel et al. (VLSI 2023)



Source: Applied Materials

APPLIED MATERIALS

Applied's Logic Innovations Enable Energy-Efficient AI



GATE-ALL-AROUND

Increases logic density up to 20% vs. FinFET

Decreases power consumption up to 30%

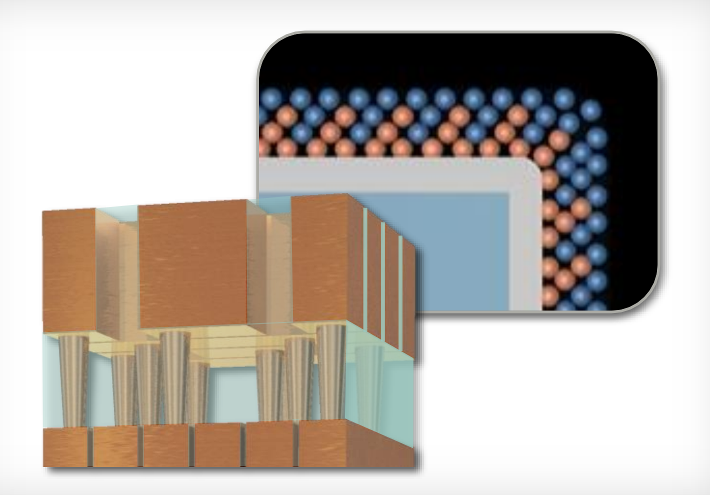
Source: Jaehun Jeong, Samsung, 2023 VLSI
FET: field effect transistor

BACKSIDE POWER DELIVERY

Increases area scaling up to 30%[1]

Decreases power consumption up to 20%[2]

Source: 1 J. Ryckaert et al., 2019 EDTM, 2 TSMC 2024 Symposium

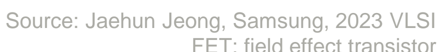


BLACK DIAMOND™ AND CuBS IMS™ WITH VOLTA™ Ru CVD

Binary liner lowers line resistance up to 25%[3]

New Black Diamond reduces chip capacitance up to 3%[4] and strengthens logic and DRAM chips for 3D stacking

Source: 3 Applied Materials, 4 Kang Sub Yim, SEC at IITC 2024
CuBS: copper barrier seed; IMS: integrated materials solution

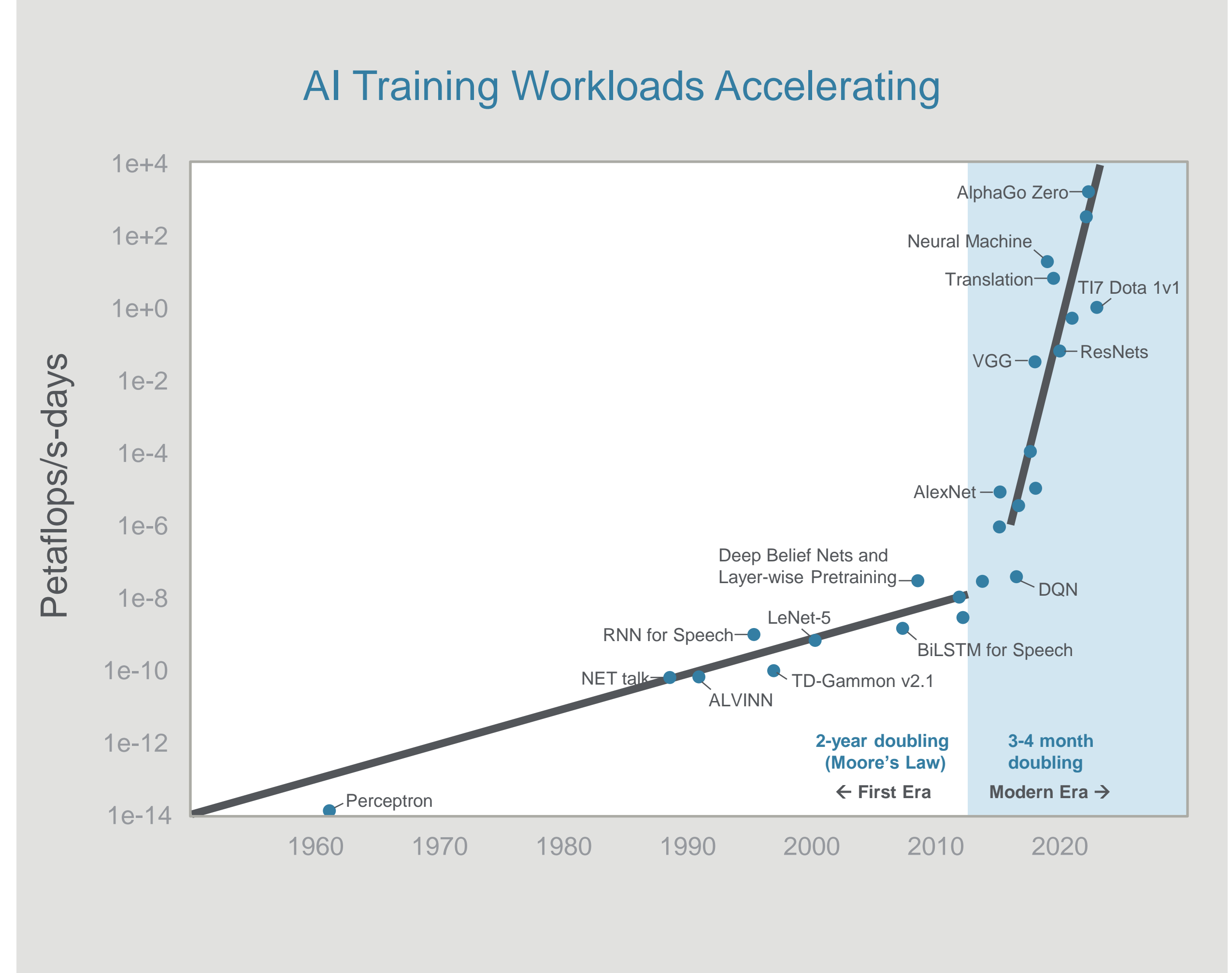


DRAM

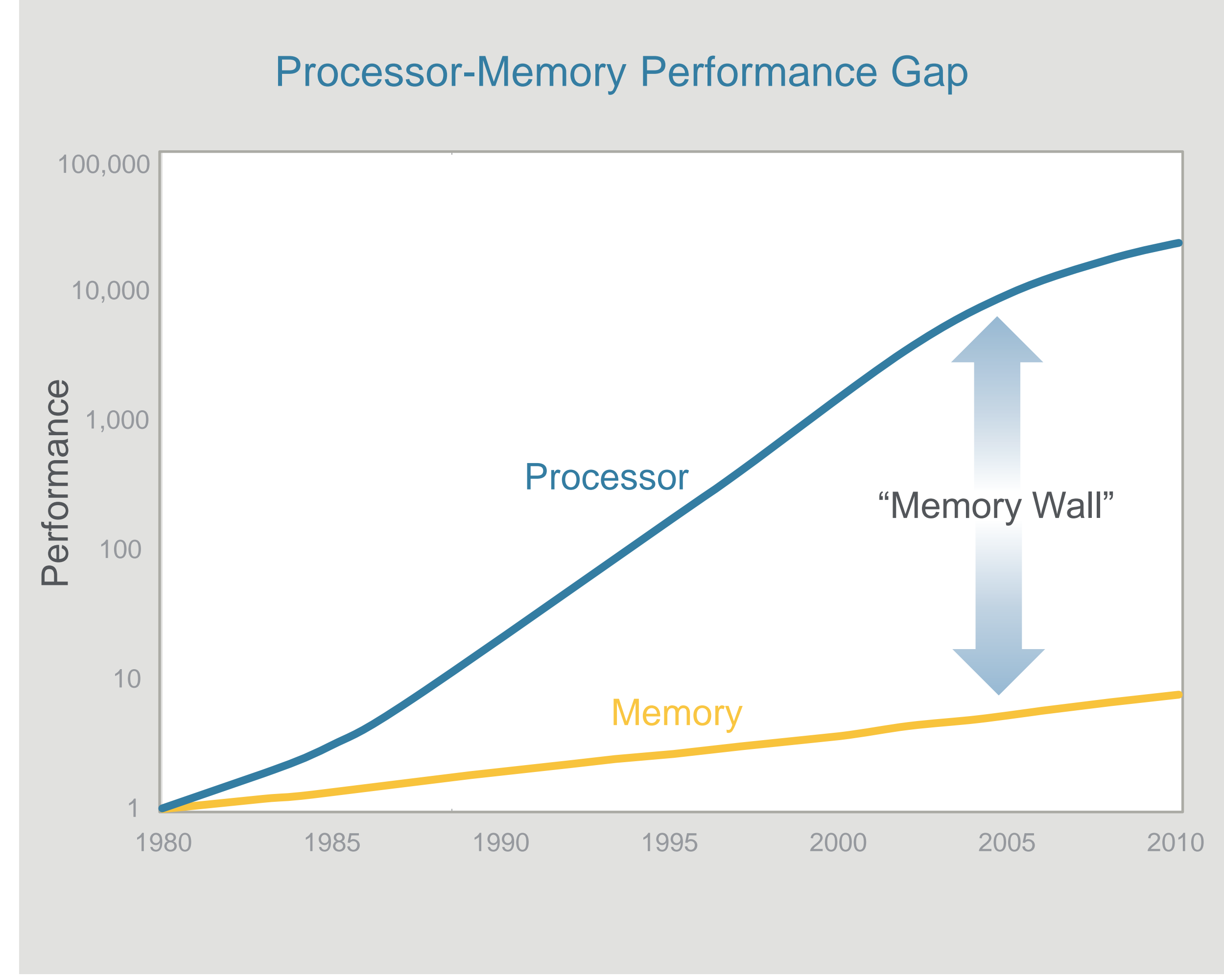
Sony Varghese, Ph.D.
Senior Director of Technical Marketing, Semiconductor Products Group

JULY 9, 2024

AI Requires Advances in Memory



Source: OpenAI, AI and Compute, 2018



Source: H. Patterson and J. Hennessy, Computer Architecture: A Quantitative Approach

DRAM Roadmap

8F2
RCAT

6F2
BCAT

4F2
VT

3D DRAM

bitline
wordline
4F
storage node contact
bit line contact
2F

2F
3F

2F
2F

RCAT: recessed channel array transistor
BCAT: buried channel array transistor
VT: vertical transistor

DRAM Scaling Levers

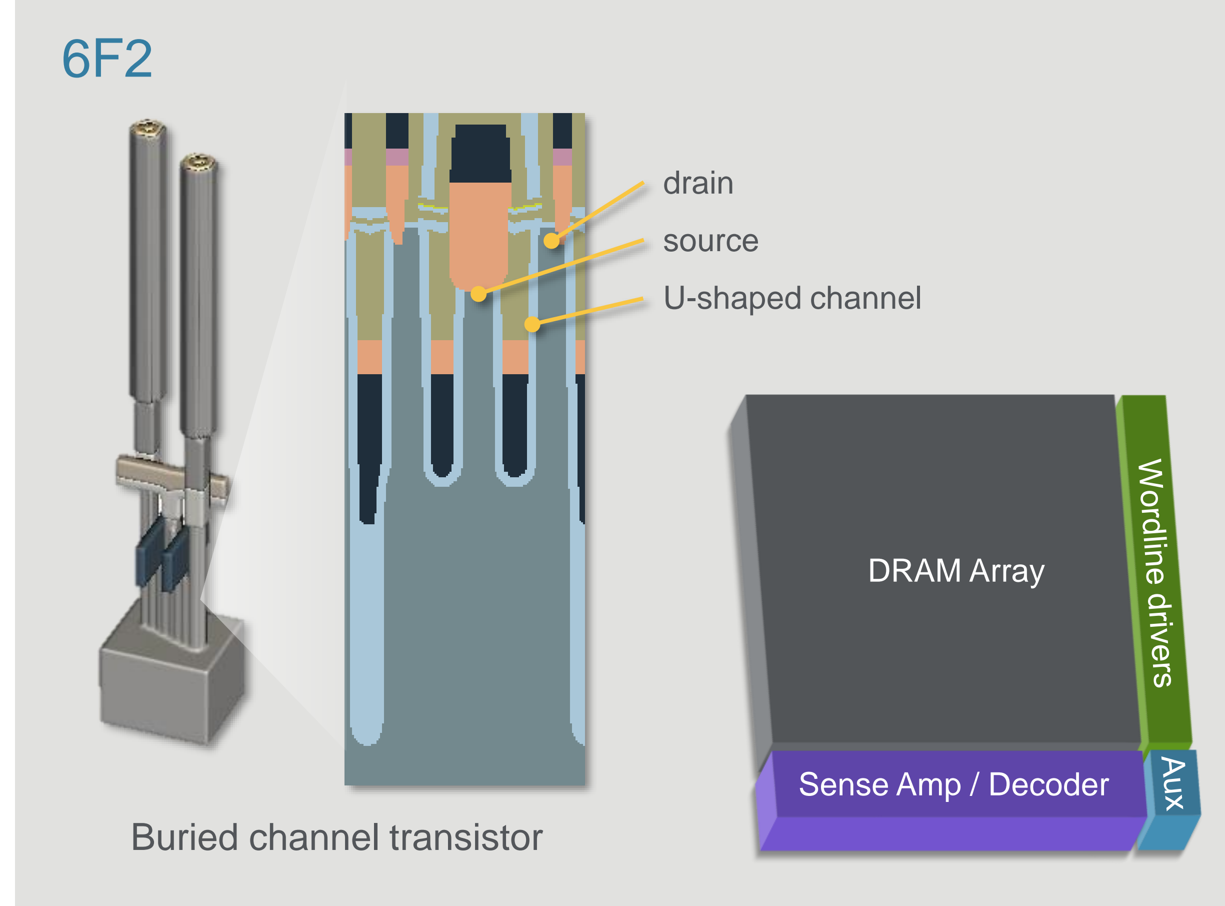
6F2
BCAT

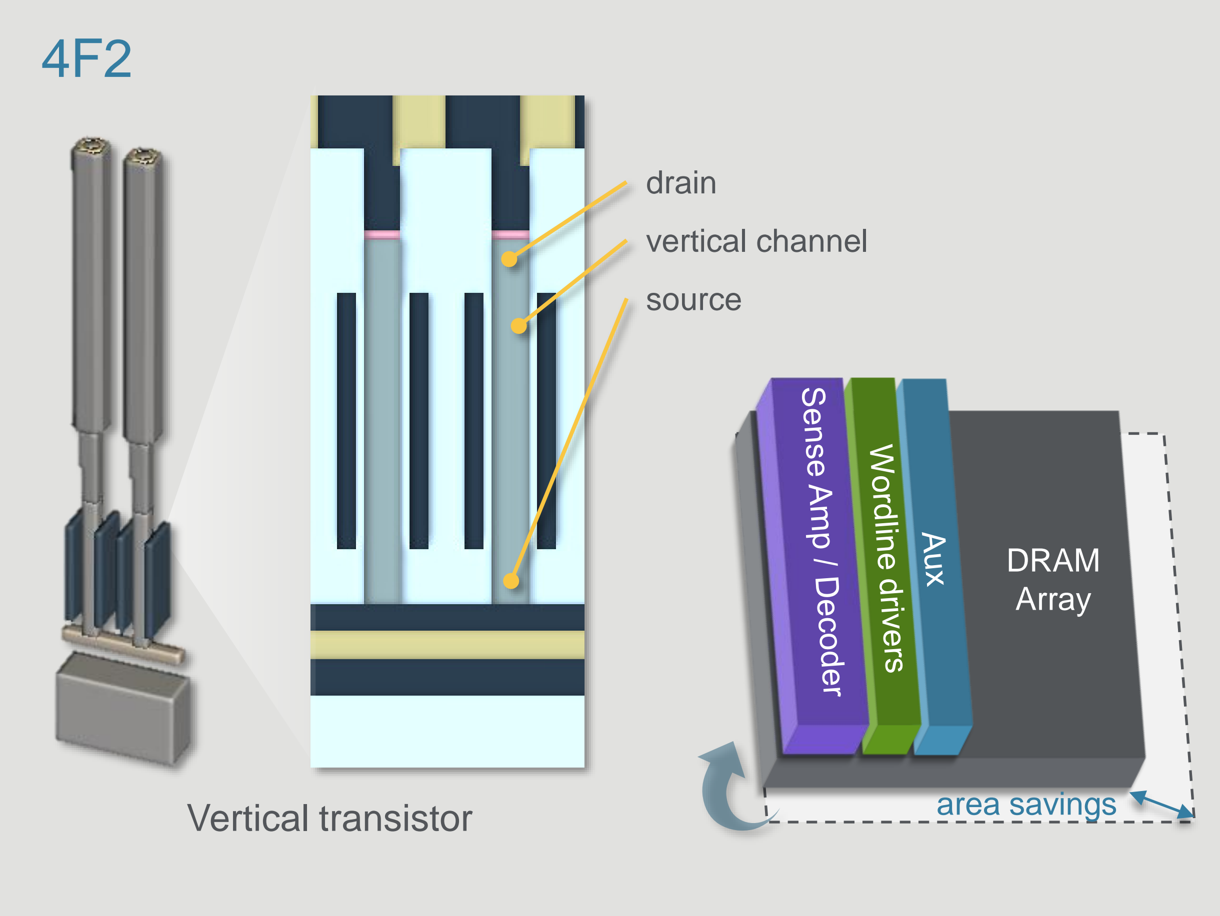
2007 – present

Scaling lever	Key modules	Current	Inflections
Cell	Capacitor Active silicon area Word line / bit line	capacitor; active area	thinner capacitors; shrinking active area
Periphery	Interconnect Transistor	dielectric film; Cu; Poly / SiON / Si: poly / SiON	Black Diamond™ Low-k + Advanced CuBS; Metal Gate / High-k / Si: HKMG

CuBS: copper barrier seed
BCAT: buried channel array transistor
HKMG: high-k metal gate

DRAM Roadmap





DTCO: Vertical transistor DRAM with wafer bonding can increase bit density by 30%

APPLIED MATERIALS.

DRAM Roadmap

8F2
RCAT

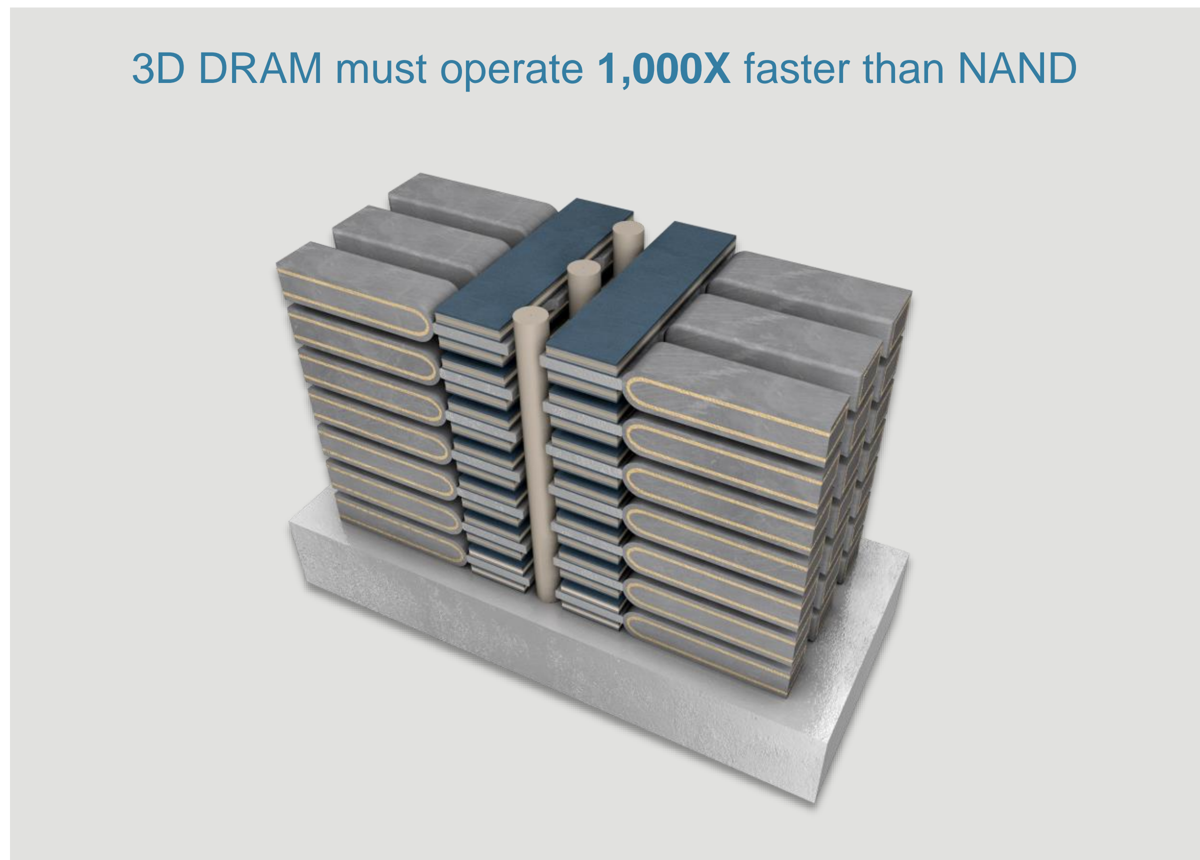
6F2
BCAT

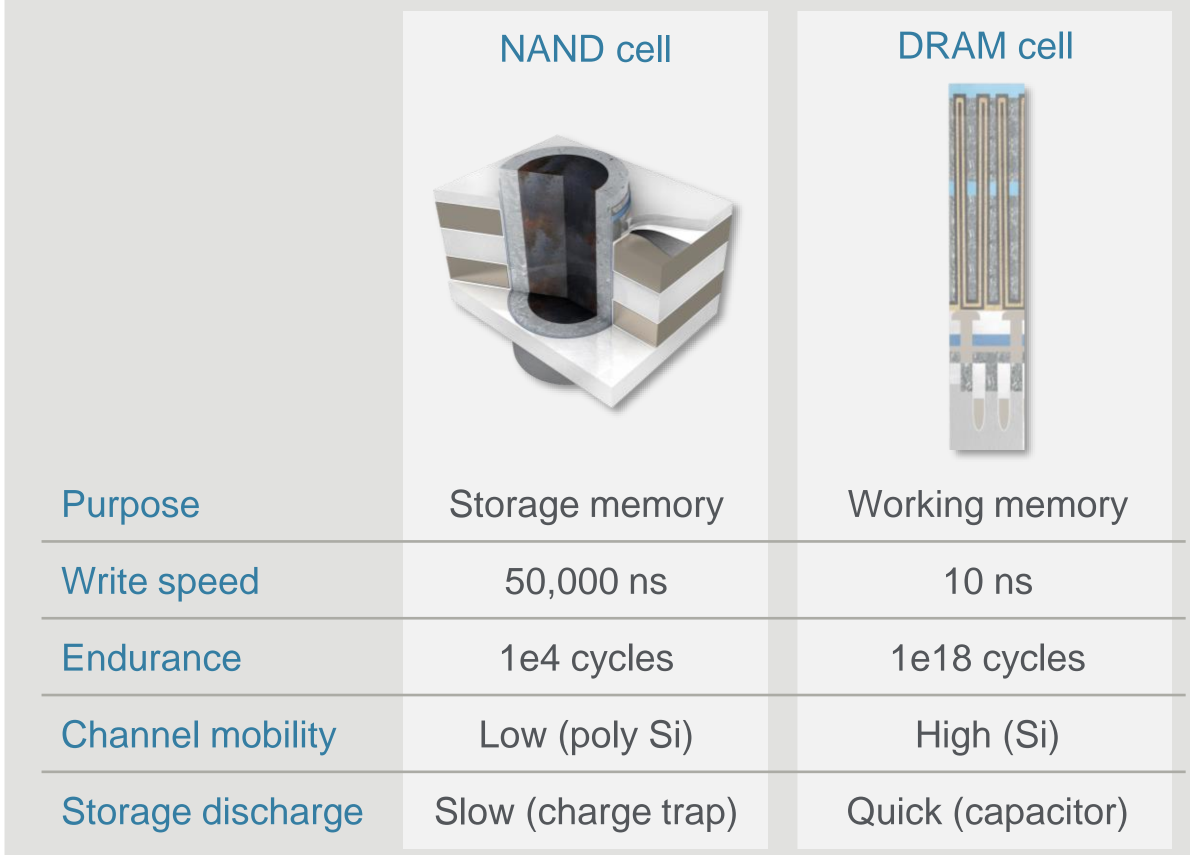
4F2
VT

3D DRAM

RCAT: recessed channel array transistor
BCAT: buried channel array transistor
VT: vertical transistor

3D DRAM Will Be Different from 3D NAND



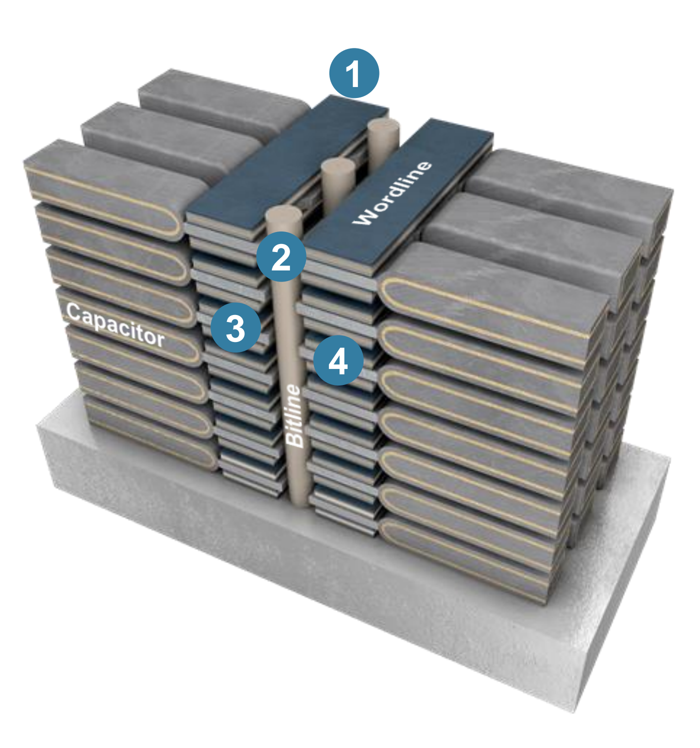


	NAND cell	DRAM cell
Purpose	Storage memory	Working memory
Write speed	50,000 ns	10 ns
Endurance	1e4 cycles	1e18 cycles
Channel mobility	Low (poly Si)	High (Si)
Storage discharge	Slow (charge trap)	Quick (capacitor)

3D DRAM will require high-mobility materials, conductor etch and selective materials removal

APPLIED MATERIALS®

Applied's Materials Engineering Capabilities for 3D DRAM



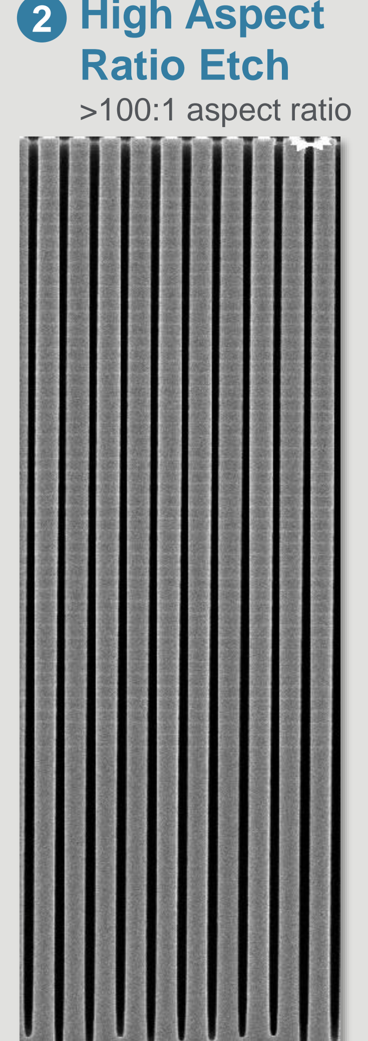
Images source: Applied Materials

1 >100 Layer Mold Stack

Si + SiGe epitaxy

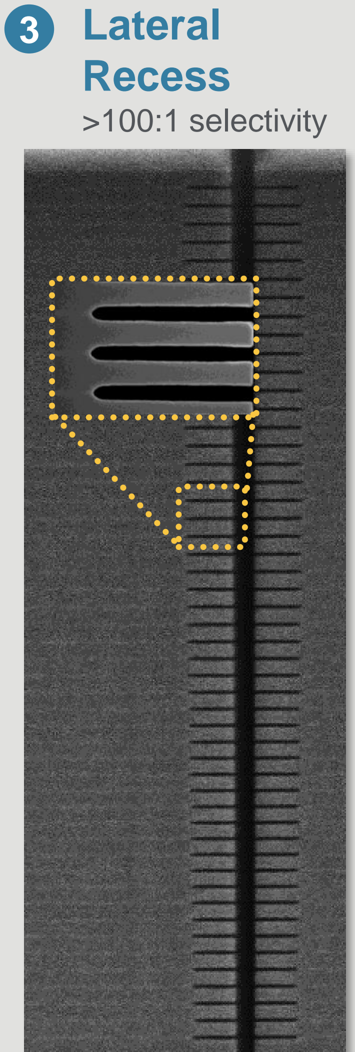
2 High Aspect Ratio Etch

>100:1 aspect ratio



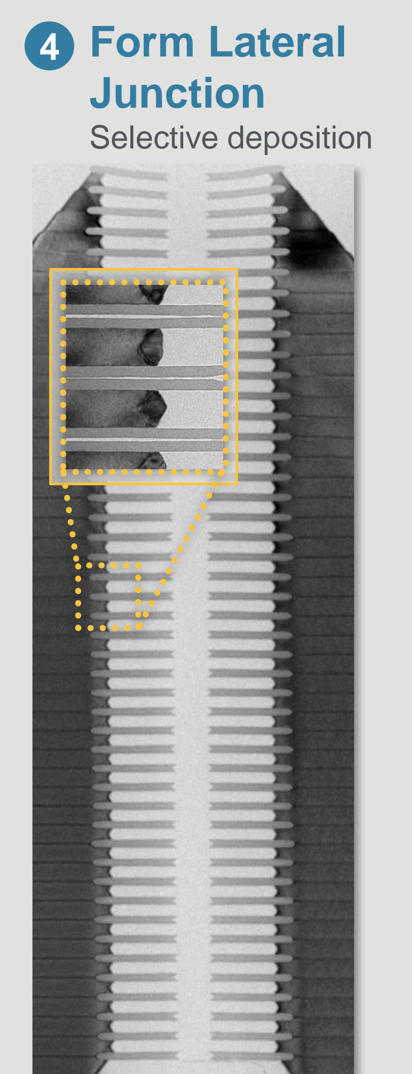
3 Lateral Recess

>100:1 selectivity



4 Form Lateral Junction

Selective deposition



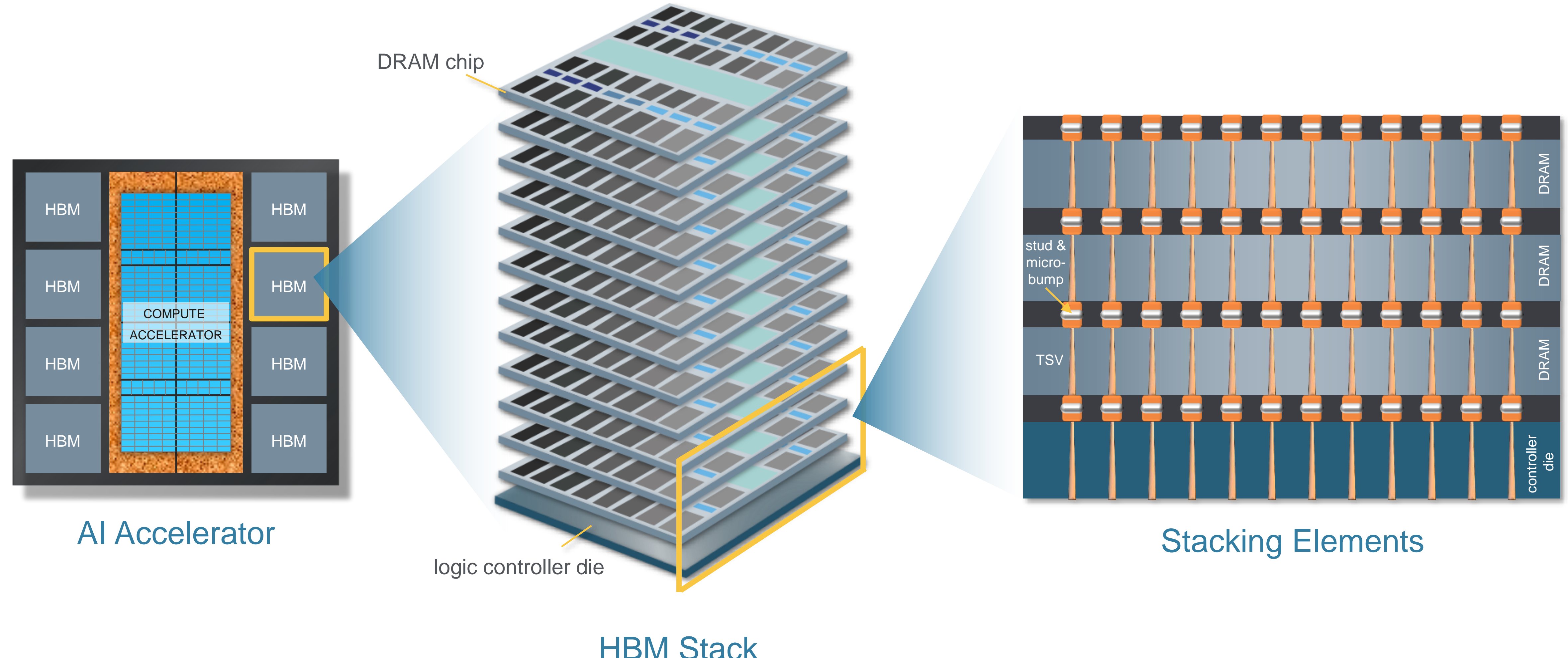
APPLIED MATERIALS®

High-Bandwidth Memory

Jinho An, Ph.D.
Account Technologist Director, Semiconductor Products Group

JULY 9, 2024

High-Bandwidth Memory



APPLIED MATERIALS

High-Bandwidth Memory: Incremental Materials Engineering Steps

DRAM Wafer

>700 steps

DRAM nodes, e.g. 1A, 1B, 1C.
Steps common for standard and HBM

Blank Wafer

Frontside

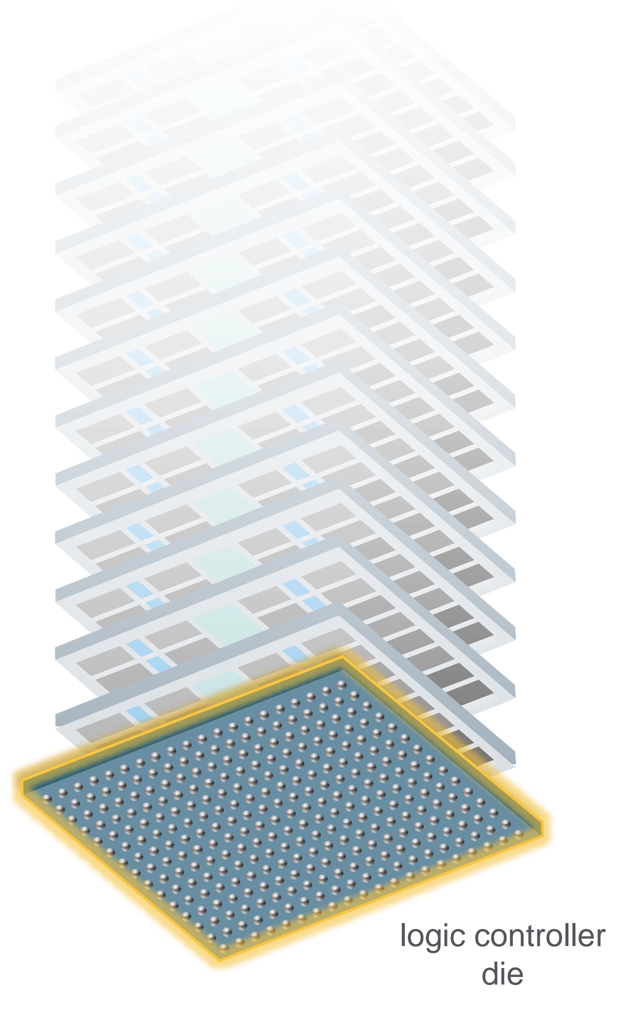
Flip, backside

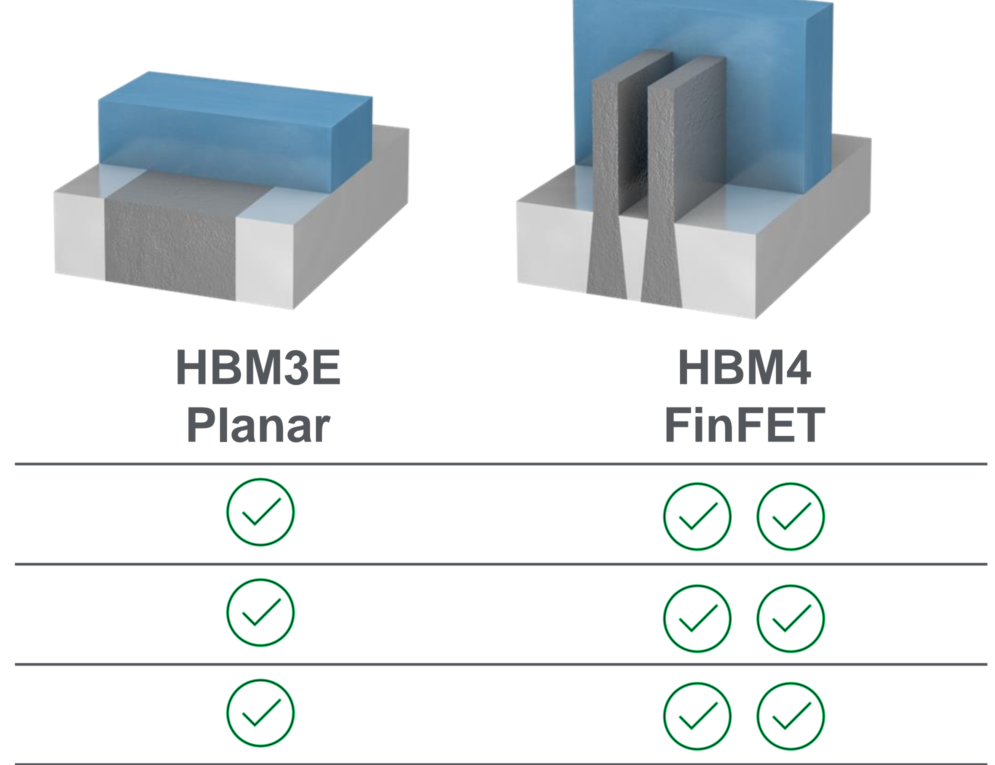
TSV Formation	TSV Etch	CVD Liner	PVD Barrier-Seed	Cu Plating	CMP
Bump (frontside)	Bond Pad Formation	PVD	Cu Plating	Resist Strip	Under-Bump Etch
TSV Reveal	Silicon Polish	Recess Etch	CVD Passivation	Cu & Oxide Polish	
Bump (backside)	Cu Expose-Develop	PVD	Cu Plating	Resist Strip	Under-Bump Etch

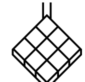
Applied's broad portfolio supports 75% of HBM materials engineering process steps
Leading in HBM with SAM share ~50%

Source: Applied Materials

High-Bandwidth Memory Controller Die

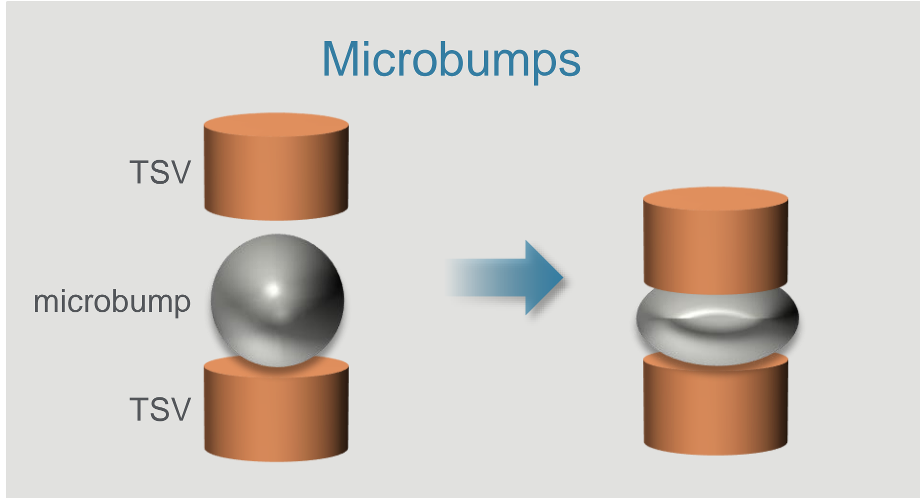


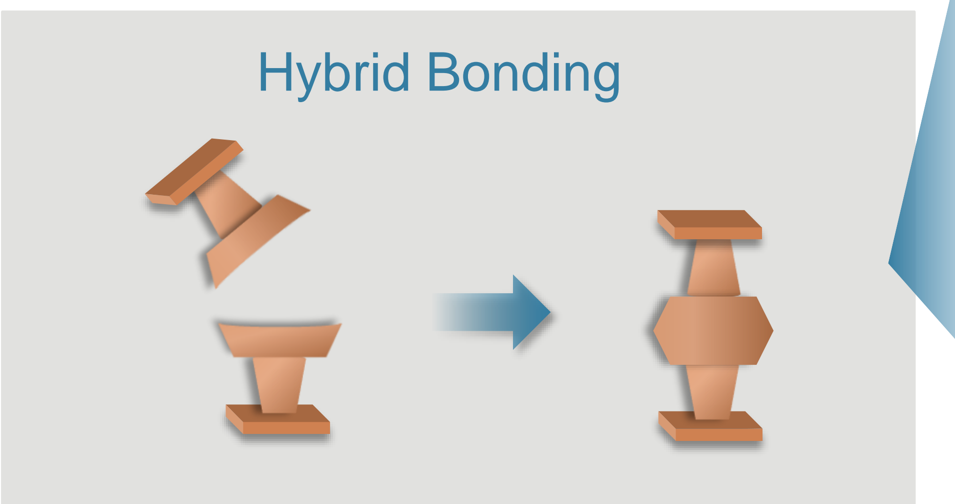


	HBM3E Planar	HBM4 FinFET
Data Transfer Speed	✓	✓ ✓
 **Transistor Density**	✓	✓ ✓
Power Consumption	✓	✓ ✓

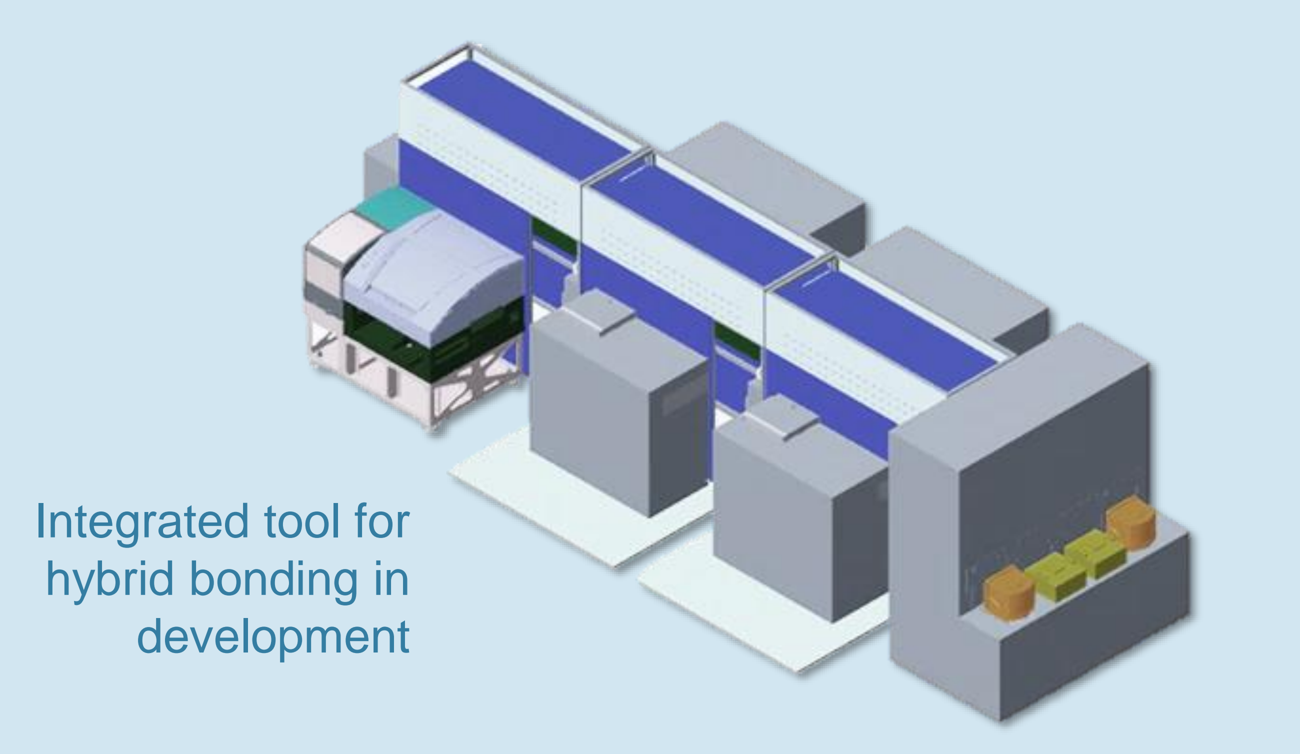
APPLIED MATERIALS®

Hybrid Bonding for High-Density Chip-to-Chip Interconnects





- 80% lower thermal resistance than microbumps
- Enables 10,000 to ~1M connections per mm^2
- Demands extreme process and alignment precision



Integrated tool for hybrid bonding in development

Source: ECTC 2024; 16H stack

Heterogeneous Integration

Sarah Wozny, Ph.D.
Director, Semiconductor Products Group

JULY 9, 2024

AI Accelerates Transition to Advanced Packaging

AI Training Workloads Accelerating

Petaflops/s-days

1e+4
1e+2
1e+0
1e-2
1e-4
1e-6
1e-8
1e-10
1e-12
1e-14

1960 1970 1980 1990 2000 2010 2020

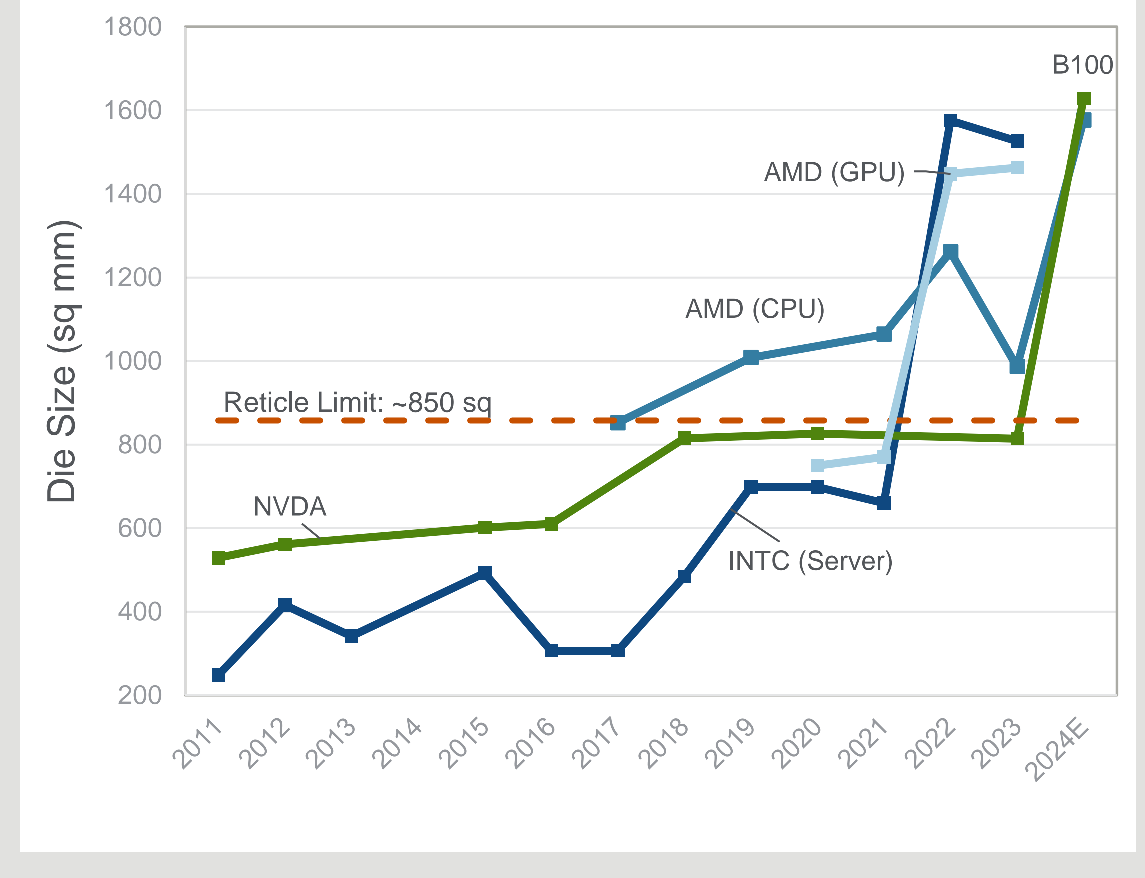
AlphaGo Zero
Neural Machine Translation
TI7 Dota 1v1
VGG
ResNets
AlexNet
Deep Belief Nets and Layer-wise Pretraining
DQN
LeNet-5
RNN for Speech
BiLSTM for Speech
NET talk
TD-Gammon v2.1
ALVINN
Perceptron

2-year doubling (Moore's Law)
← First Era

3-4 month doubling
Modern Era →

Source: OpenAI, "AI and Compute" 2018

Server Die Sizes Increasing Beyond Reticle Limit

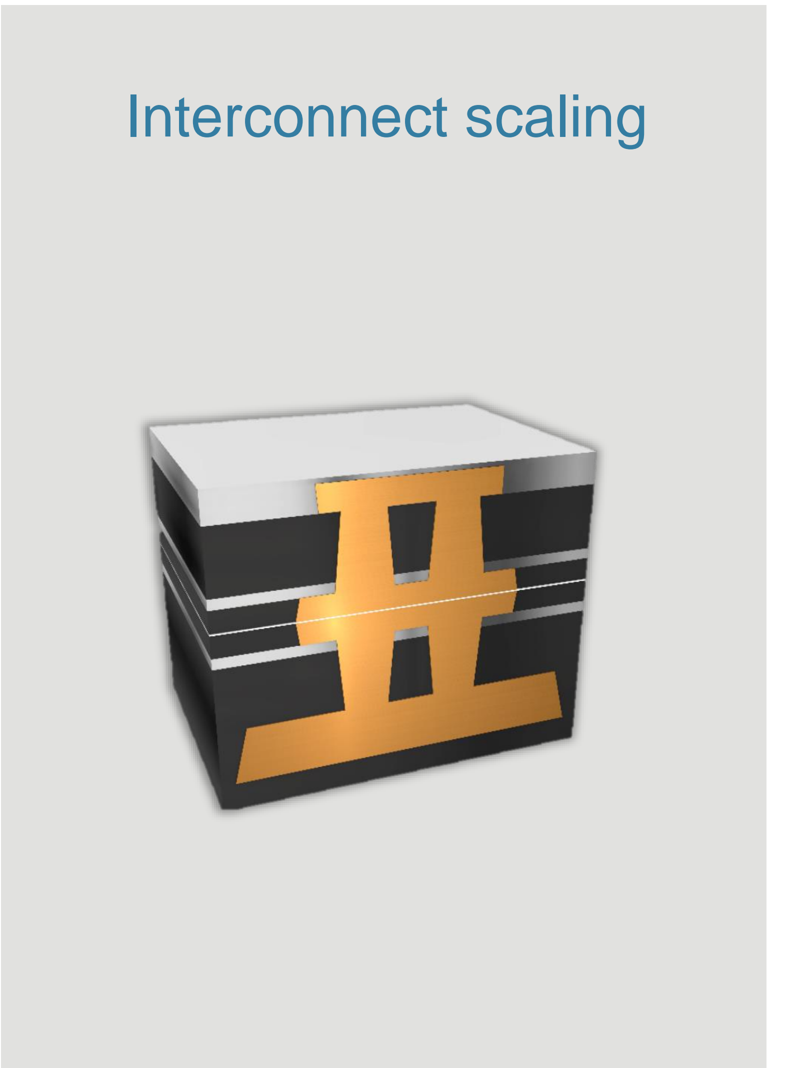


Source: Evercore ISI Research, Anandtech, wccftech.com, techpowerup.com, Locuza

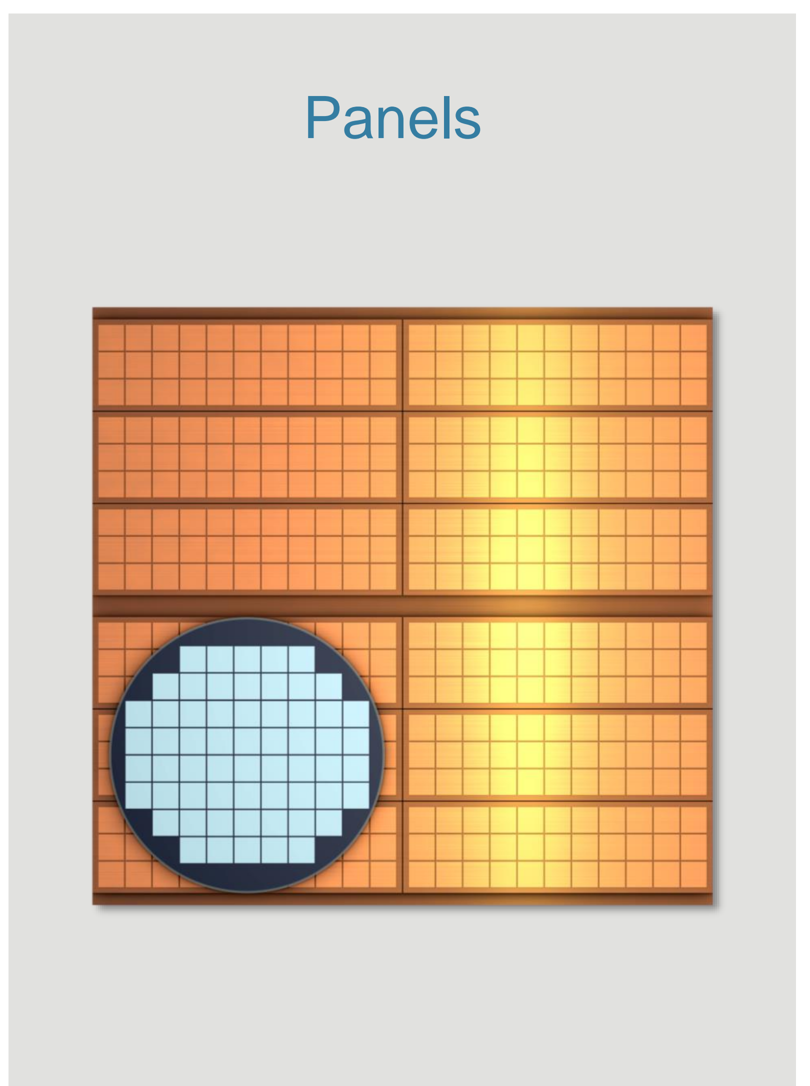
Advanced Packaging Roadmap Drivers

Die stacking

Interconnect scaling

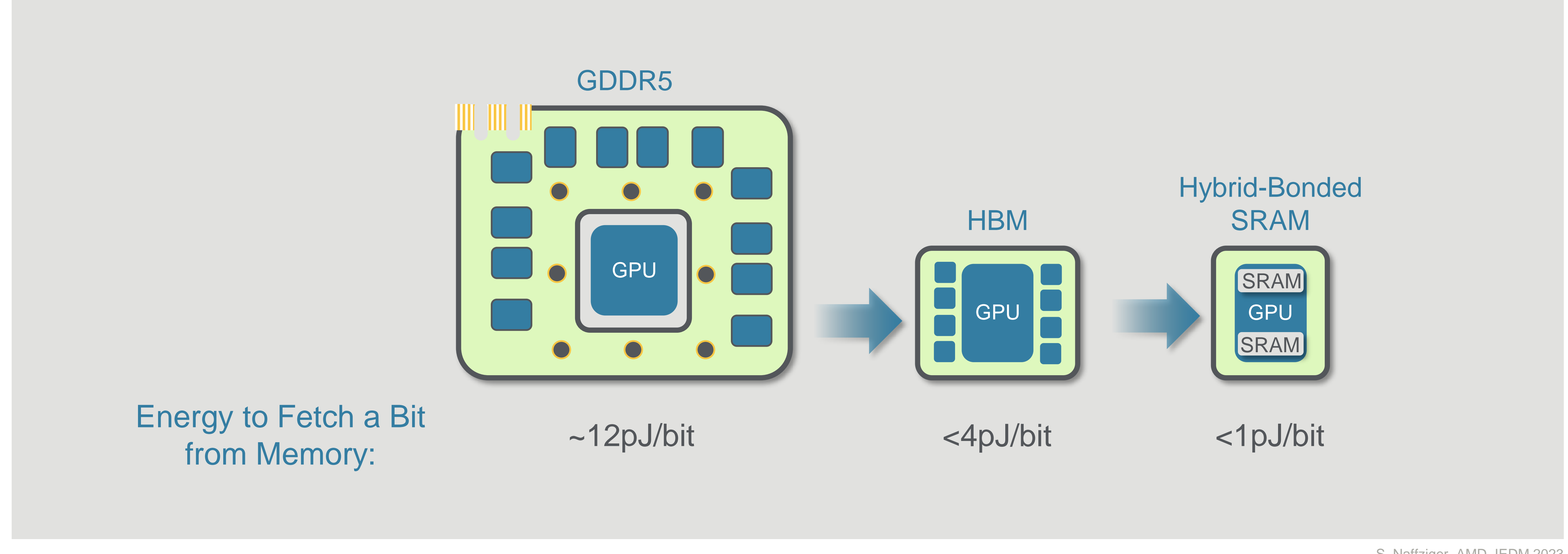


Panels



APPLIED MATERIALS

Localizing Memory Reduces Power Consumption



S. Naffziger, AMD, IEDM 2023

APPLIED MATERIALS

Packaging System Interconnect Scaling Roadmap

I/O density (finer pitch)

Wire Bond

< 10 I/O / mm²
> 10 pJ / bit

Bump to PCB

< 100 I/O / mm²
> 1.5 pJ / bit

Microbumps
(chip stacking)

< 1,000 I/O / mm²
> 0.5 pJ / bit

Through-Silicon Vias
(chip stacking)

< 10,000 I/O / mm²
> 0.1 pJ / bit

Hybrid Bonding
(chiplet stacking)

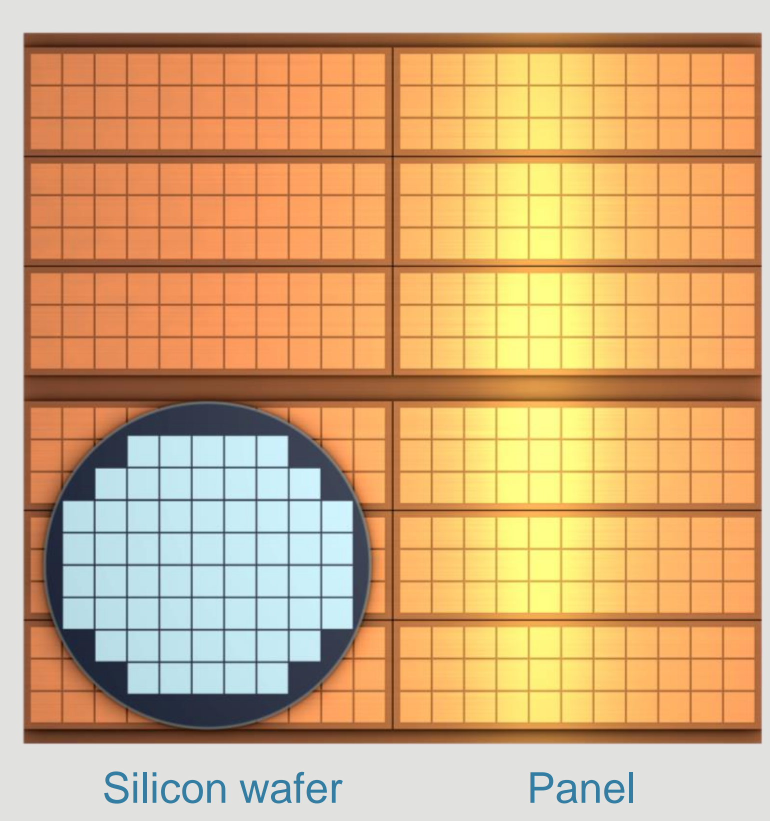
10,000 to ~1M I/O / mm²
Power: <0.05 pJ / bit

Power efficiency (lower interconnect length)

PCB: printed circuit board, I/O: input/output, pJ: picojoules

APPLIED MATERIALS

Panel Processing Enables Larger Packages for AI



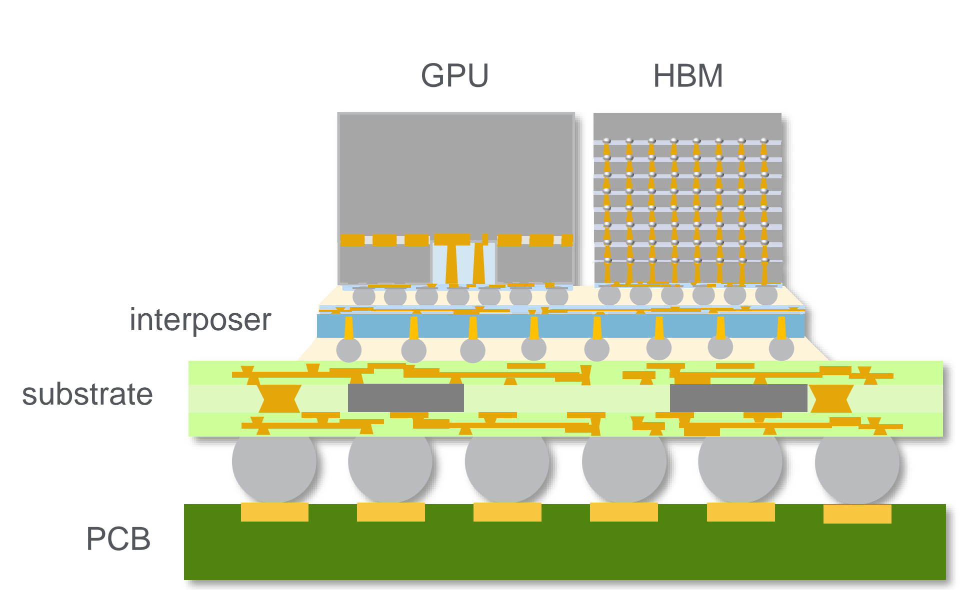
Silicon wafer
300mm diameter

Panel
510x515mm

- Round wafers have poor area efficiency
- Panels enable packages as large as 10,000mm^2

Source: Applied Materials

Glass Enables Larger and Faster Packages for AI



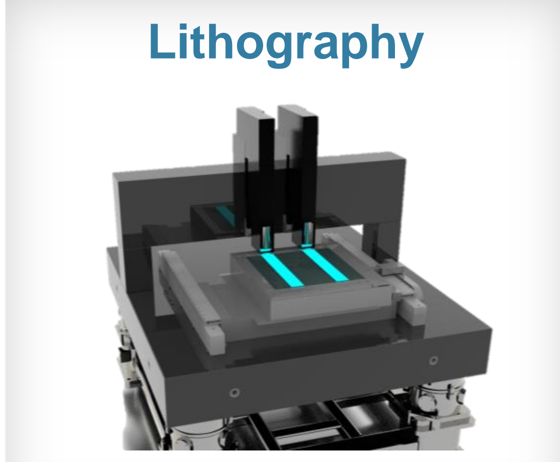
AI Package Requirements	Material Properties	Glass	Organic
Larger Packages	Mechanical stiffness	6X	1X
	Thermal expansion	0.1X	1X
Faster Signal Propagation	Loss tangent	4X	1X

Source: Adapted from Yole Intelligence, Status of the Advanced IC Substrate Industry 2023
PCB: printed circuit board; GPU: graphical processing unit; HBM: high-bandwidth memory

APPLIED MATERIALS

Applied is Accelerating the Panel Ecosystem

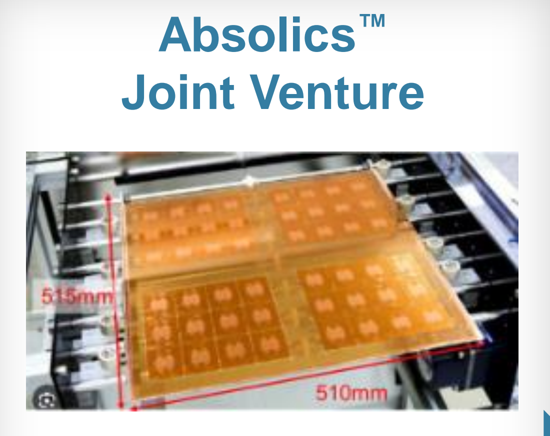
Lithography



Deposition

Test

Absolics™ Joint Venture



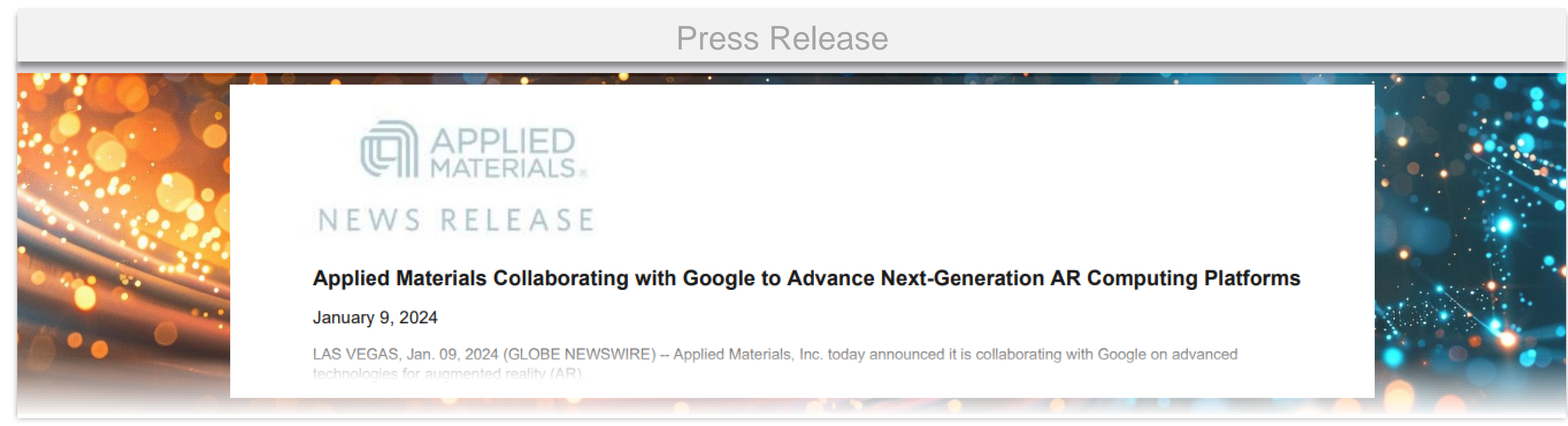
Applied leveraging its front-end process technologies and display expertise for panel packaging

Lithography	Deposition	Test	Absolics™ Joint Venture
Maskless digital lithography for sub-2-micron patterning	Topaz™ for panels up to 600mm X 600mm	eBeam test technology proven in the LCD industry	Glass panel manufacturing in the U.S.

APPLIED MATERIALS

High-Performance Photonics Platform at Scale

Press Release


APPLIED MATERIALS

NEWS RELEASE

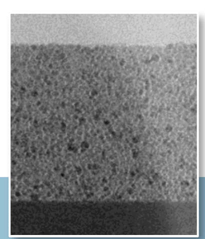
Applied Materials Collaborating with Google to Advance Next-Generation AR Computing Platforms

January 9, 2024

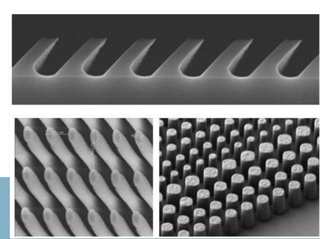
LAS VEGAS, Jan. 09, 2024 (GLOBE NEWSWIRE) -- Applied Materials, Inc. today announced it is collaborating with Google on advanced technologies for augmented reality (AR).

Modeling and Design

Advanced Materials



Process Capabilities



Metrology and Inspection

Scale-Up and Automation

Glasses Prototyping

Applied's Photonics Materials-to-Systems Platform

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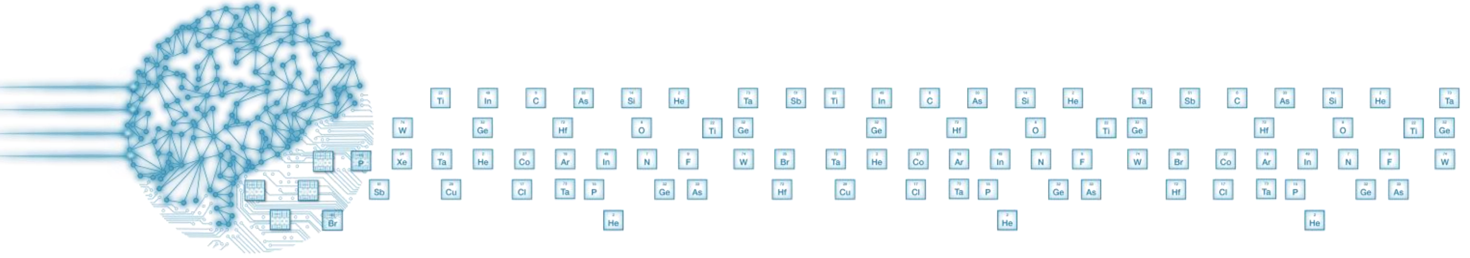
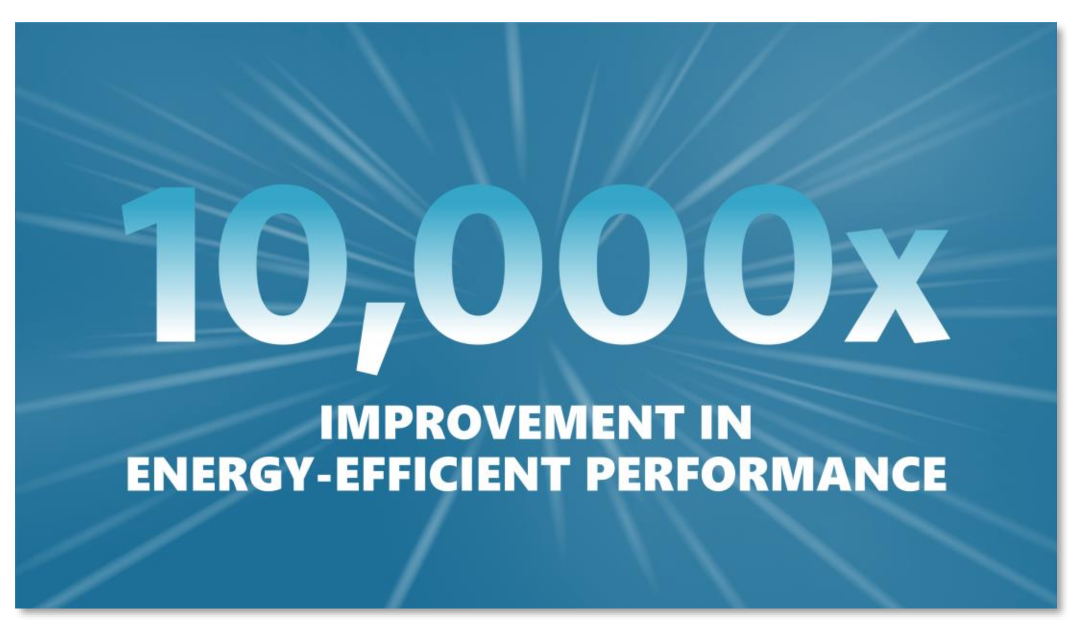
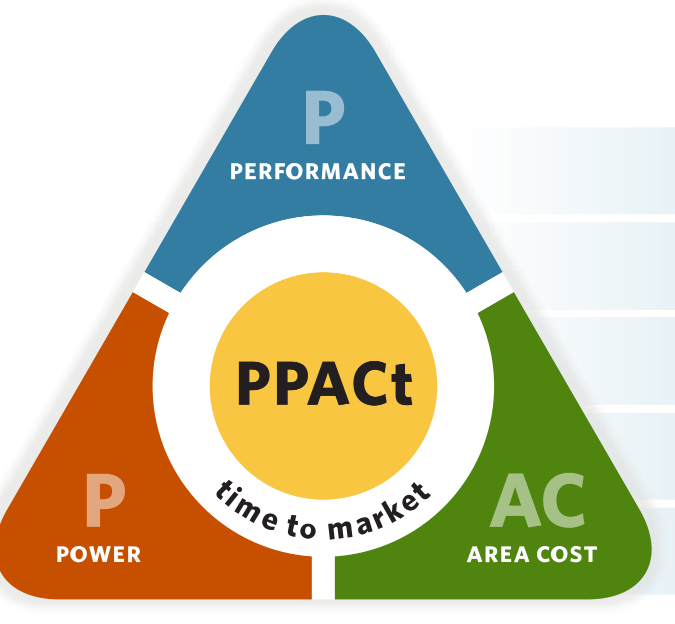
AI Design Forum™ 2018

Tuesday, July 10, Yerba Buena Theater, SF



Gary Dickerson
CEO
Applied Materials





ENABLED BY

- New architectures
- New structures / 3D
- New materials
- New ways to shrink
- Heterogeneous integration

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Growing Our Opportunity and Share

Prabu Raja, Ph.D.
President, Semiconductor Products Group

JULY 9, 2024

The Race for AI Leadership – Fueled by Materials Engineering

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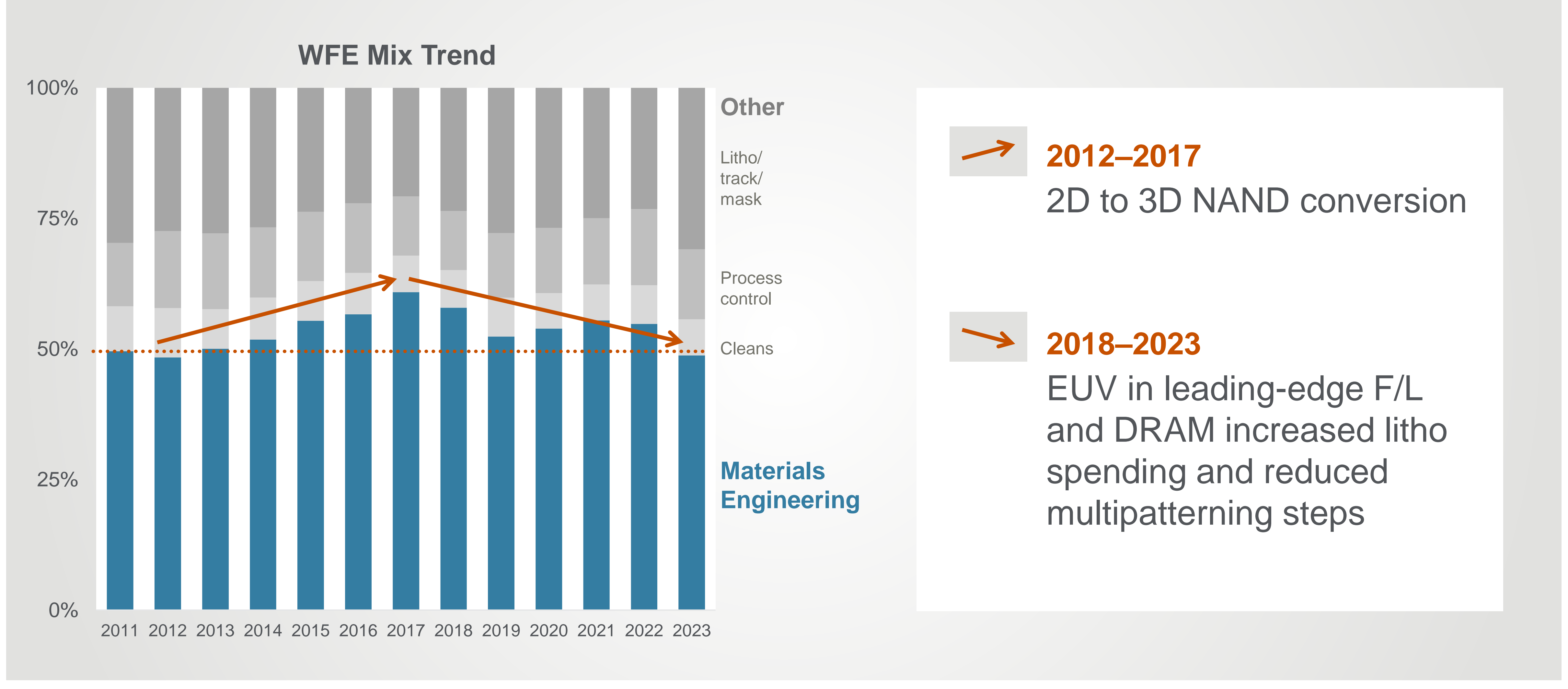
Materials Engineering Has Been ~50% or More of WFE



Source: Gartner (2011-19), TechInsights (2020-23), Applied Materials analysis. Materials Engineering is creating and depositing materials; shaping and removing materials; modifying materials; and connecting chips with advanced packaging. The related equipment categories are deposition (MOCVD, ECD/other, CVD, Epi PVD), modification (Implant, Thermal) and removal (CMP, etch). Materials Engineering excludes litho/track/mask, process control and cleans.

Applied Has Gained Share in Materials Engineering and WFE

WFE Mix Trend

Applied Materials Positions

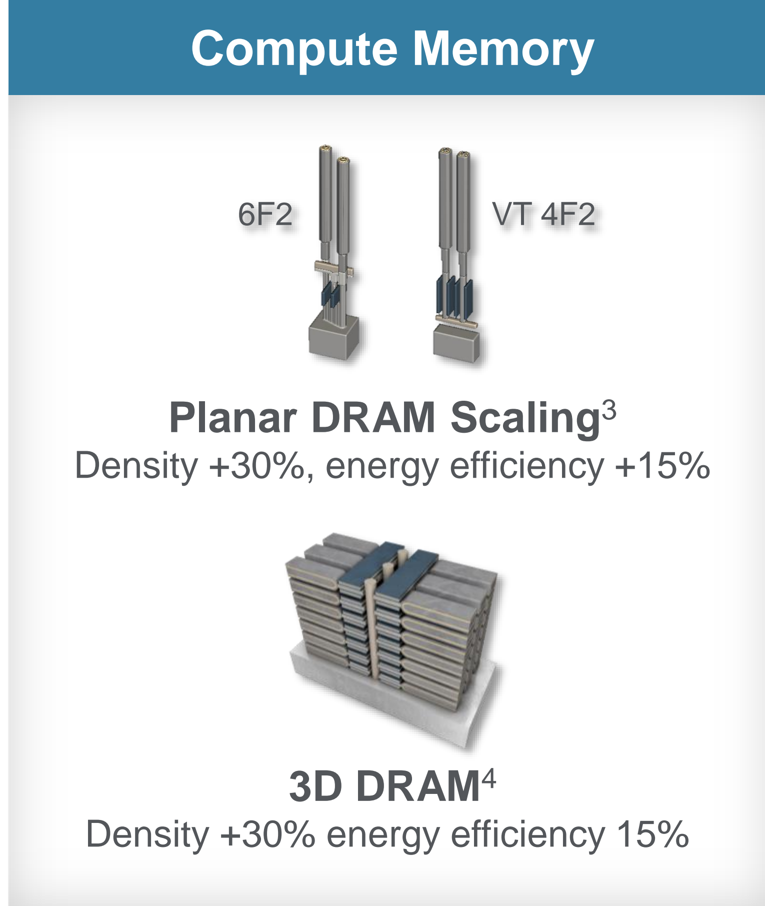
Source: Gartner (2011-19), TechInsights (2020-23), Applied Materials analysis. Materials Engineering is creating and depositing materials; shaping and removing materials; modifying materials; and connecting chips with advanced packaging. The related equipment categories are deposition (MOCVD, ECD/other, CVD, Epi PVD), modification (Implant, Thermal) and removal (CMP, etch). Materials Engineering excludes litho/track/mask, process control and cleans.

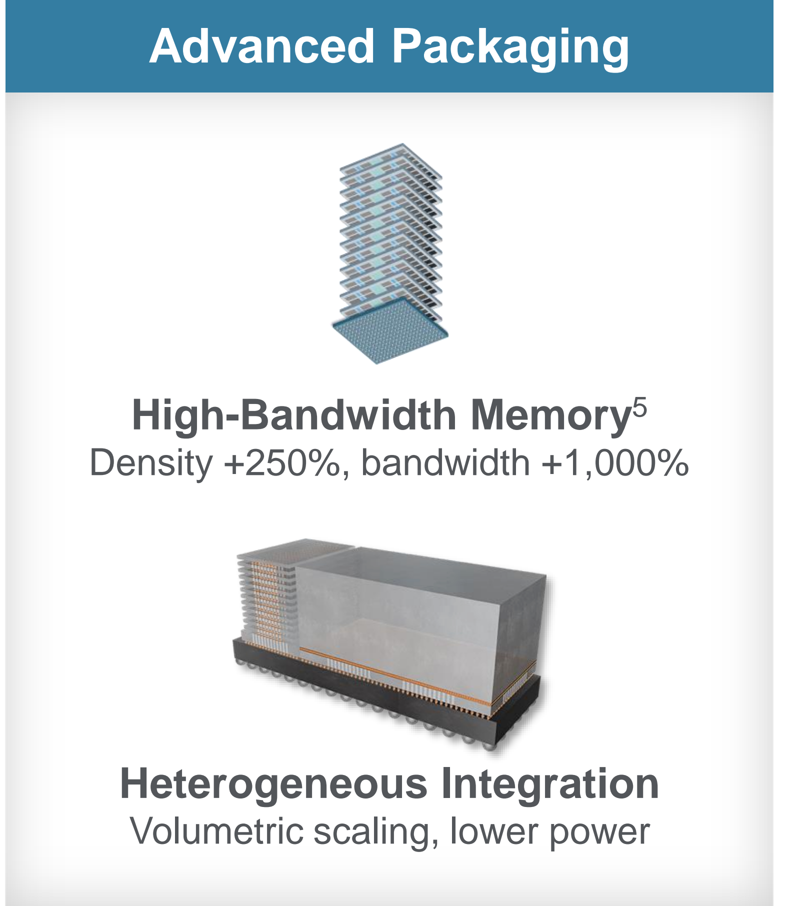
Materials Engineering-Enabled Technology Inflections

High-Performance Logic

Gate-All-Around[1]
Density +20%, energy efficiency +30%

Backside Power Delivery[2]
Density +30%, energy efficiency +20%





Helping deliver 10,000X improvement in energy-efficient performance by 2040[6]

1. Jaehun Jeong, Samsung 2023 VLSI; 2. IEEE Explore 2019; TSMC 2024 Symposium; 3. Applied Materials estimates node over node
4. Applied Materials 3D DRAM vs. last generation of 4F2; 5. Applied Materials HBM3E vs. GDDR6X; 6. IEEE Spectrum, “How We’ll Reach a 1 Trillion Transistor GPU”

Expect Materials Engineering to Increase within WFE Mix

Materials Engineering vs. Litho/Track WFE Mix*

100%

0%

Litho/Track

Materials Engineering

	LOGIC						DRAM					
	20nm+	16/14nm	7nm	5/4nm	3nm	GAA+BPD	D1a	D1b	D1c	D1d	VT 4F2	3D DRAM
Materials engr % of **incremental** WFE*	>50%	>40%	>40%	>60%	>75%			>60%	>70%	>40%	>100%	>100%

Source: Applied Materials analysis

* Materials engineering vs litho/track WFE mix & ME as % of incremental WFE exclude cleans and process control

Materials engineering (ME) % of incremental WFE = (ME WFE spend on new node – ME WFE spend on prior node) / (WFE spend on new node – WFE spend on prior node)

Materials Engineering Inflections Increase Applied's Opportunity

Applied's 2023 Market Share

SHARE BY DEVICE

Total WFE share	21.6%
Leading-edge F/L	**~21%**
ICAPS	~23%
DRAM	**~23%**
NAND	<15%

2023 Total WFE = $95.7B

Advanced Packaging	
WFE share	~30%
SAM share	~50%
SAM share of HBM	~50%

2023 advanced packaging WFE = ~$3.9B (included in other devices)

Expect Inflections to be Accretive to SAM and SAM Share

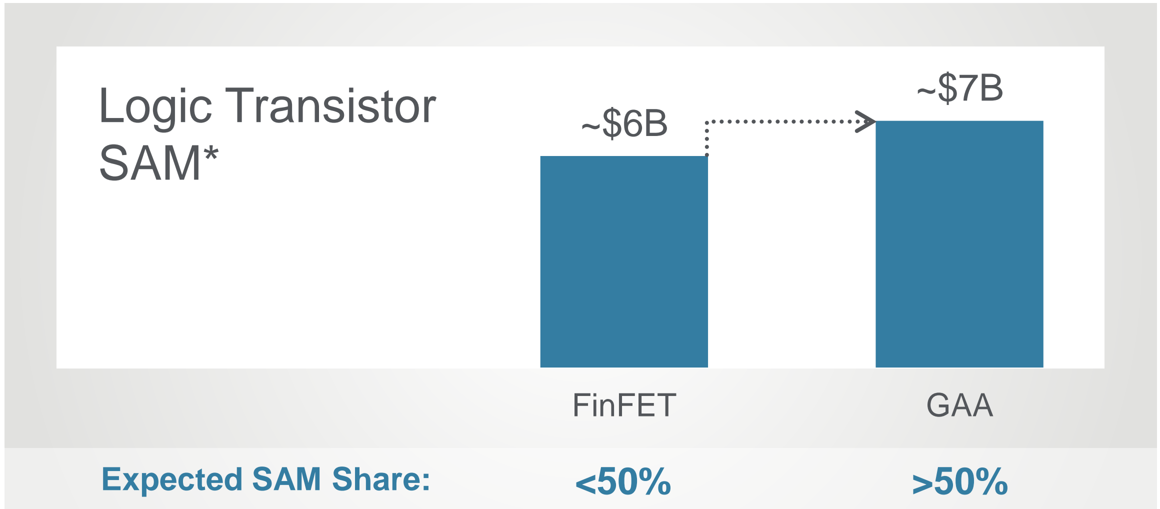
	TRANSISTOR		+ WIRING		= TOTAL SAM	
	FinFET →	GAA	Frontside →	Frontside + Backside	FinFET, no backside wiring →	GAA + backside wiring
SAM*	$6B	$7B	$6B	$7B	$12B	$14B
SAM share	<50%	>50%	>50%	>50%		

	DRAM SCALING		
	6F2 →	VT 4F2 →	3D DRAM
SAM	$6.0B	$6.5B	$7.5B
SAM share	<50%	~50%	>50%

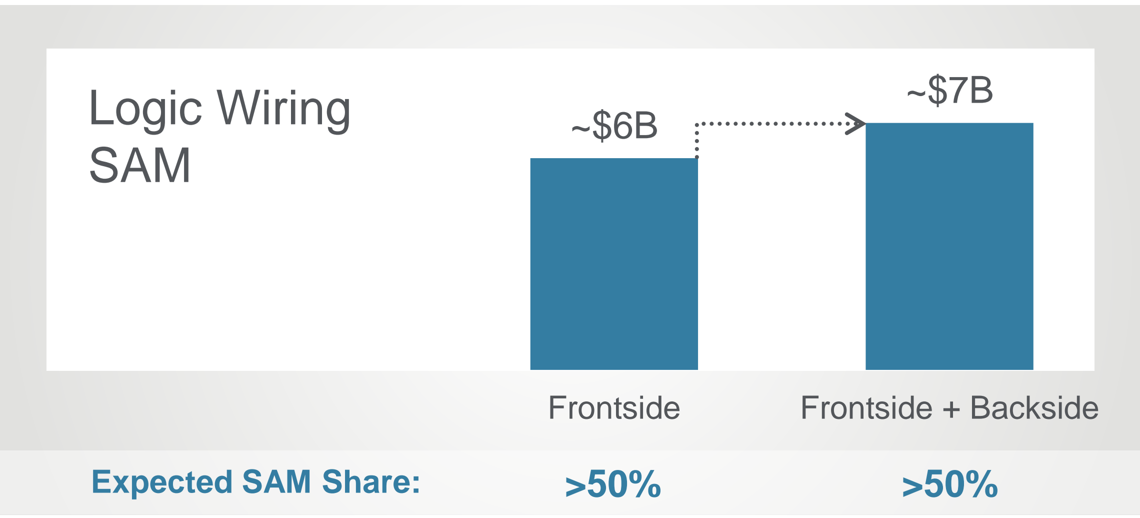
	HIGH-BANDWIDTH MEMORY	
	TSV + µbump →	TSV + hybrid bonding
SAM	~$450M	~$600M
SAM share	~50%	>50%

* Per 100k wafer starts per month capacity. SAM = Served Addressable Market
Source: TechInsights, Applied Materials analysis. Sizing is based on current estimates of customer process implementations
ICAPS = Internet of Things, Communications, Automotive, Power, Sensors; includes F/L spending at 10nm and above nodes.

Advanced Logic Growth Opportunities



Expected SAM Share:	<50%	>50%



Expected SAM Share:	>50%	>50%

- Unique connected portfolio of materials engineering technologies
- Incremental steps add ~$2B SAM to Applied's leadership segments

GAA

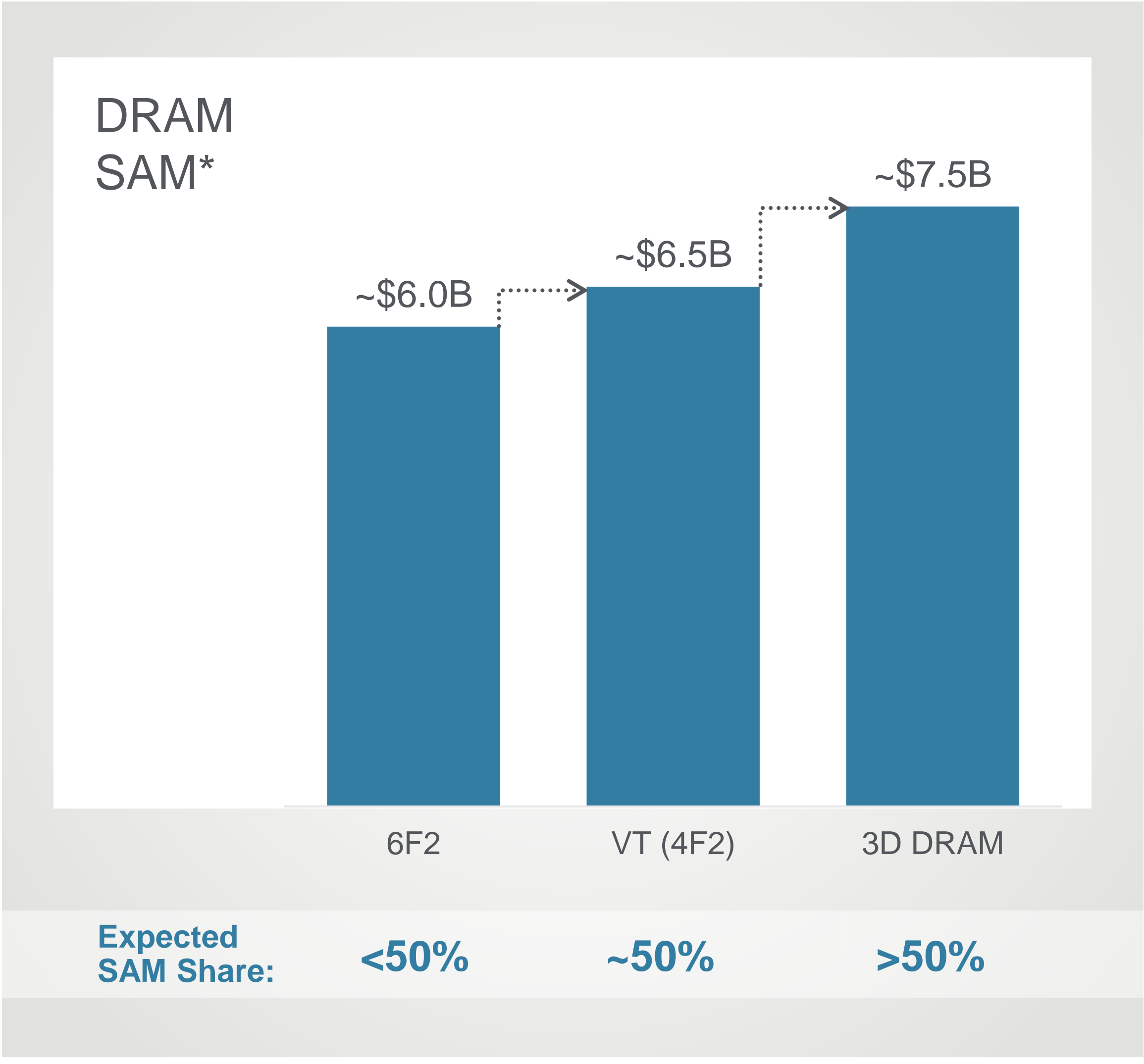
- ALD
- CMP
- CVD
- Epitaxy
- Etch
- Implant
- Process Control
- PVD
- Selective Removal
- Thermal Processes

BPD

- ALD
- CMP
- CVD
- Epitaxy
- Etch
- Process Control
- PVD

Per 100k wafer starts per month capacity. SAM = Served Addressable Market
GAA: gate all around, BDP backside power delivery

DRAM Growth Opportunities



Vertical Transistor (4F2)

- Materials engineering steps increase
- Uses Applied's leadership transistor and packaging technologies
- Bonding of DRAM cell and periphery CMOS wafers increases Applied's opportunity

3D DRAM

- Further increase in materials engineering intensity
- Uses Applied's leadership in high-mobility materials, conductor etch and selective materials removal

* Per 100k wafer starts per month capacity. SAM = Served Addressable Market

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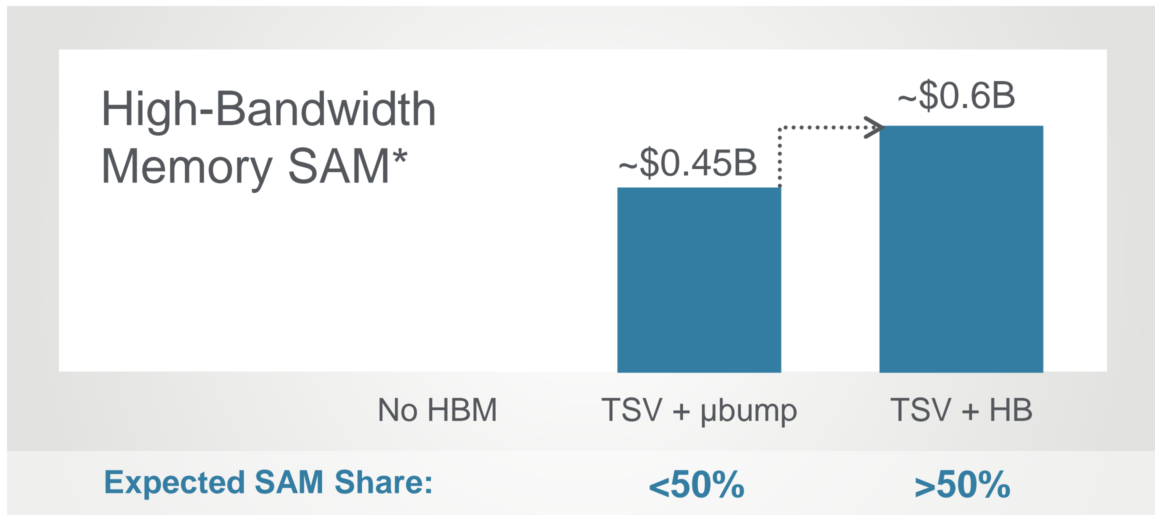
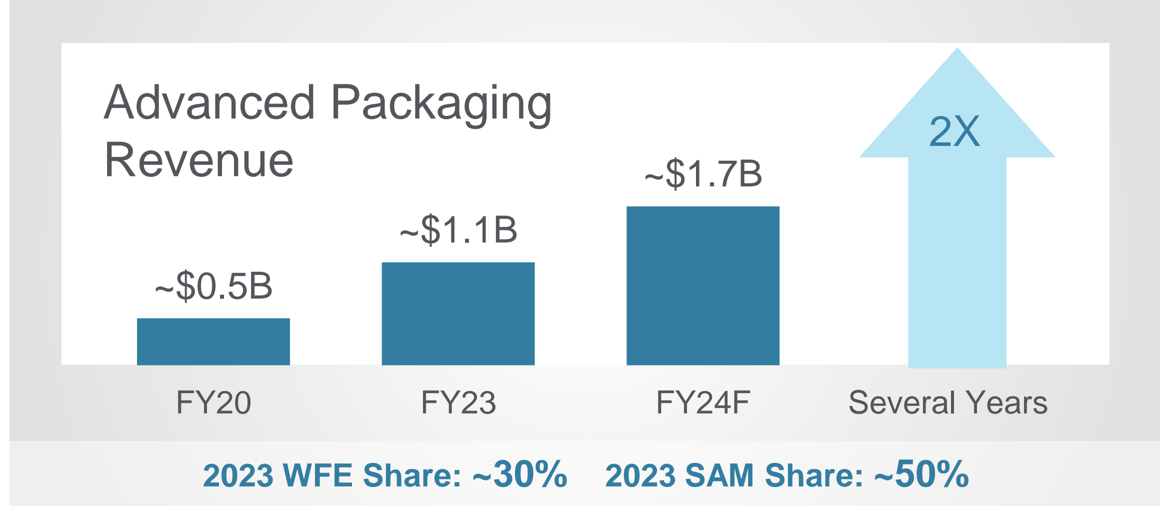
Packaging Growth Opportunities





Industry's broadest and most connected heterogeneous integration portfolio:

High-Bandwidth Memory

» Serve 14 of 19 ME steps in TSV + µbump

» Hybrid bonding increases SAM and share

Advanced Packaging

» Extends Applied's leadership in wiring to a fast-growing new market

» Building a leadership portfolio for emerging hybrid bonding and panel technologies

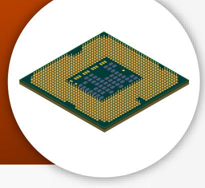
» Applied's display expertise helps accelerate panel ecosystem

* Per 100k wafer starts per month capacity. SAM = Served Addressable Market

Applied's AI-Fueled Growth Thesis

Global GDP

Semiconductors



Wafer Fab Equipment

Applied Semi Systems

Applied Global Services

1. **Semiconductors** significantly outgrow GDP
2. **Fab equipment** grows as fast or faster than semiconductors
3. **Applied Semi Systems** outgrows fab equipment market
4. **Applied Global Services** grows as fast or faster than Semi Systems

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2024 SEMICON WEST TECHNOLOGY BREAKFAST