APPLIED MATERIALS®
make possible

New Ways to Shrink

EXTENDING CLASSIC MOORE'S LAW SCALING AND APPLYING DTCO

MASTER CLASS
April 21, 2022

Forward-Looking Statements and Other Information

Today's presentations contain forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, our business forecast beyond fiscal 2021, the impact of the ongoing COVID-19 pandemic and responses thereto on our operations and financial results, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; global economic and industry conditions; the effects of regional or global health epidemics, including the severity and duration of the ongoing COVID-19 pandemic; global trade issues and changes in trade and export license policies, including rules and interpretations promulgated by U.S. Department of Commerce expanding export license requirements for certain products sold to certain entities in China; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; acquisitions, investments and divestitures; changes in income tax laws; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

Use of Non-GAAP Adjusted Financial Measures

Applied provides investors with certain non-GAAP adjusted financial measures, which assume certain tax rate and weighted average shares of Applied common stock outstanding in future periods. Management uses these non-GAAP adjusted financial measures for planning purposes. Applied believes these measures enhance an overall understanding of its projected future performance. There are limitations in using non-GAAP financial measures because they are not prepared in accordance with generally accepted accounting principles, may be different from those used by other companies, and may exclude or include certain items that may have a material impact upon our reported financial results. The presentation of this additional information is not meant to be considered in isolation or as a substitute for the directly comparable financial measures prepared in accordance with GAAP.

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2022 MASTER CLASSES

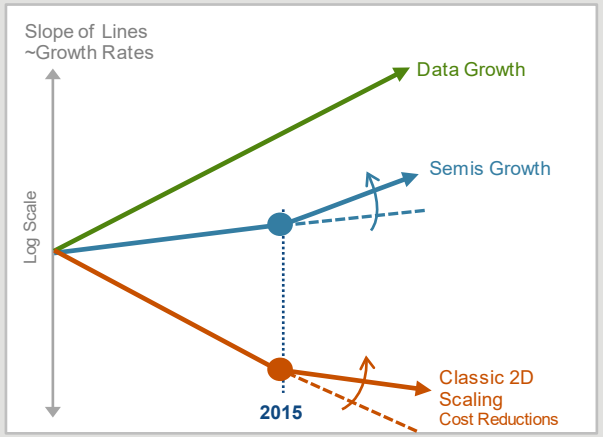
WELCOME

Michael Sullivan
Corporate Vice President
Head of Investor Relations

NEW WAYS TO SHRINK MASTER CLASS | April 21, 2022

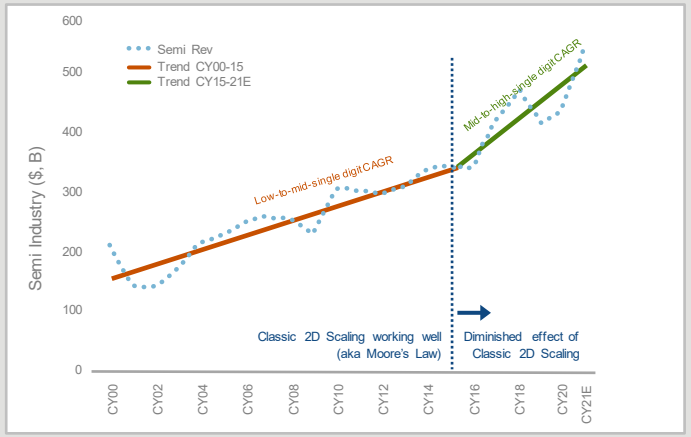
“Battle of Exponential” Blog Series

Battle of Exponentials Inflection



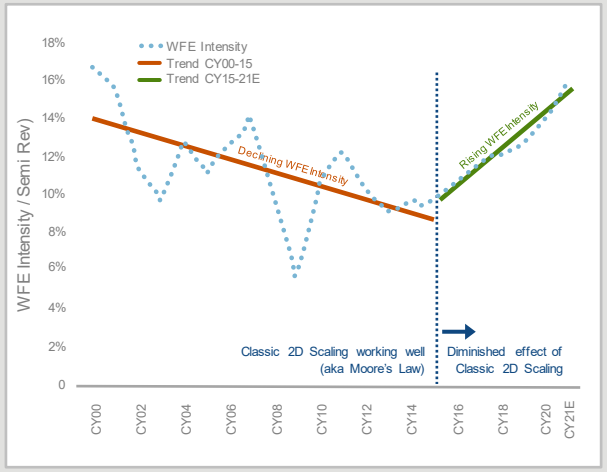
Source: Applied Materials – Strategy & Market Intelligence

Semiconductor Revenue Growth Inflection



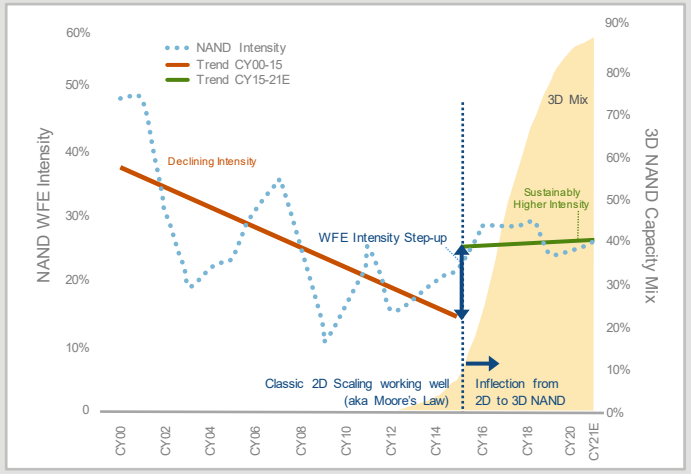
Source: SIA, SEMI, TechInsights (VLSI research), Applied Materials – Strategy & Market Intelligence

WFE Intensity Inflection



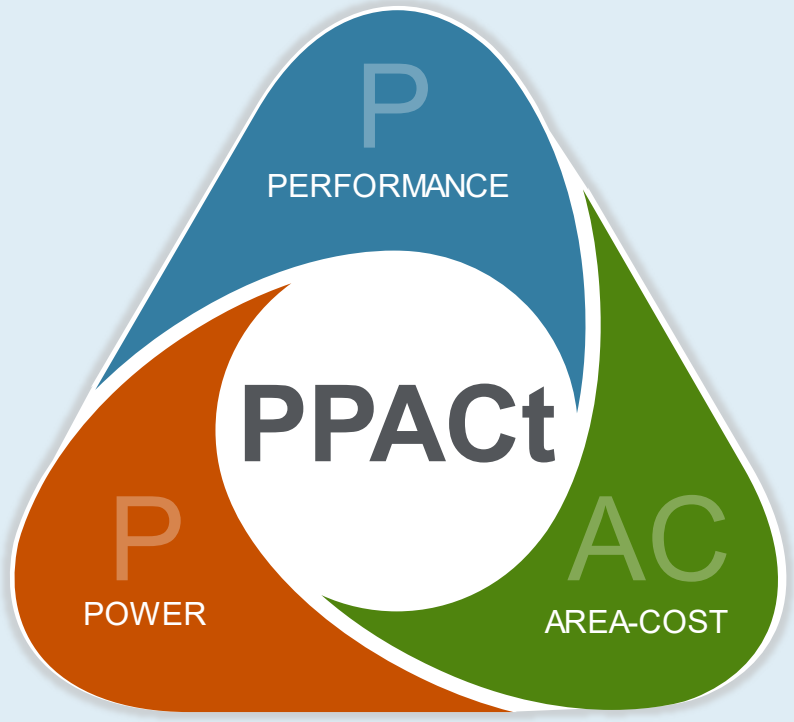
Source: Applied Materials – Strategy & Market Intelligence

NAND WFE Intensity Inflection



Source: Applied Materials – Strategy & Market Intelligence

The New Playbook



Enabled by	Key Inflections
New architectures	▪ New ASICs and accelerators ▪ New memory / in-memory compute ▪ Specialty, CIS, power
New structures / 3D	▪ GAA transistors ▪ Backside power distribution ▪ 3D NAND, 3D DRAM
New materials	▪ Gate ▪ Contact ▪ Interconnect
New ways to shrink	▪ EUV enablement ▪ Materials-enabled patterning
Advanced packaging	▪ High-bandwidth memory ▪ 2.5D silicon interposer ▪ 3D TSV, hybrid bonding
Time to market	▪ Process control ▪ AI^{x}™

CIS: CMOS Image Sensors
GAA: Gate-All-Around
EUV: Extreme Ultraviolet
TSV: Through Silicon Via

2024 Financial Model

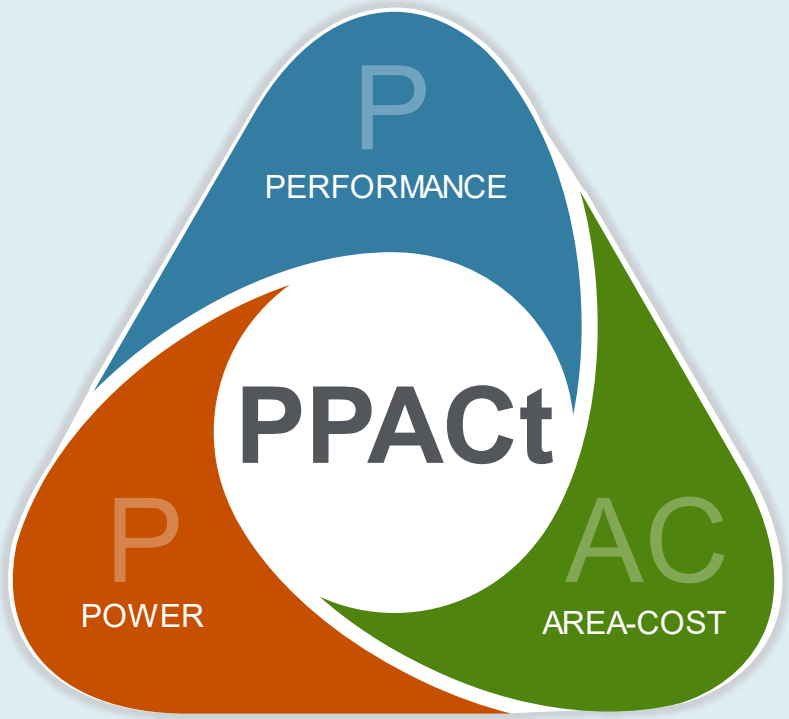
		FY'20	FY'24 MODEL		
			LOW	BASE	HIGH
	Revenue	**$17.2B**	**$23.4B**	**$26.7B**	**$31.0B**
	Semi Systems	$11.4B	$16.2B	$18.4B	$21.7B
	Services	$4.2B	$5.6B	$6.1B	$6.7B
	Display	$1.6B	$1.6B	$2.2B	$2.7B
NON-GAAP ADJUSTED*	**GM%**	**45.1%**	**47.5%**	**48.5%**	**48.8%**
NON-GAAP ADJUSTED*	**OP%**	**26.3%**	**30.6%**	**32.4%**	**32.7%**
NON-GAAP ADJUSTED*	**EPS**	**$4.17**	**$7.00**	**$8.50**	**$10.00**

2024 model assumes non-GAAP adjusted tax rate of 12.0% and weighted average shares of 875M.
*Assumes non-GAAP adjustments as applicable for future periods. For reconciliation of GAAP to non-GAAP measures, see appendix of this presentation.

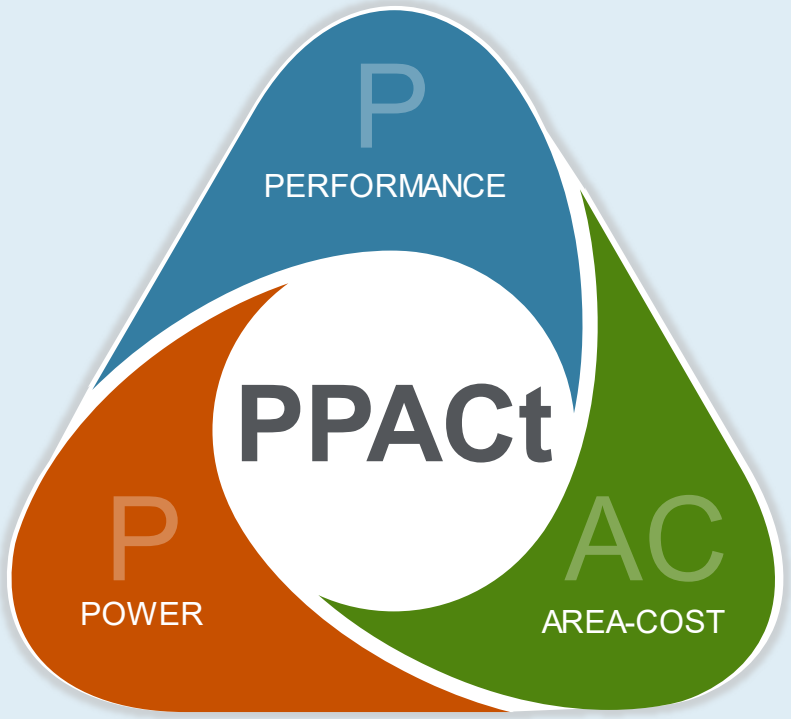
2022 Master Classes

APRIL 21

New Ways to Shrink



New Playbook for Power, Performance, Area-Cost and Time to Market



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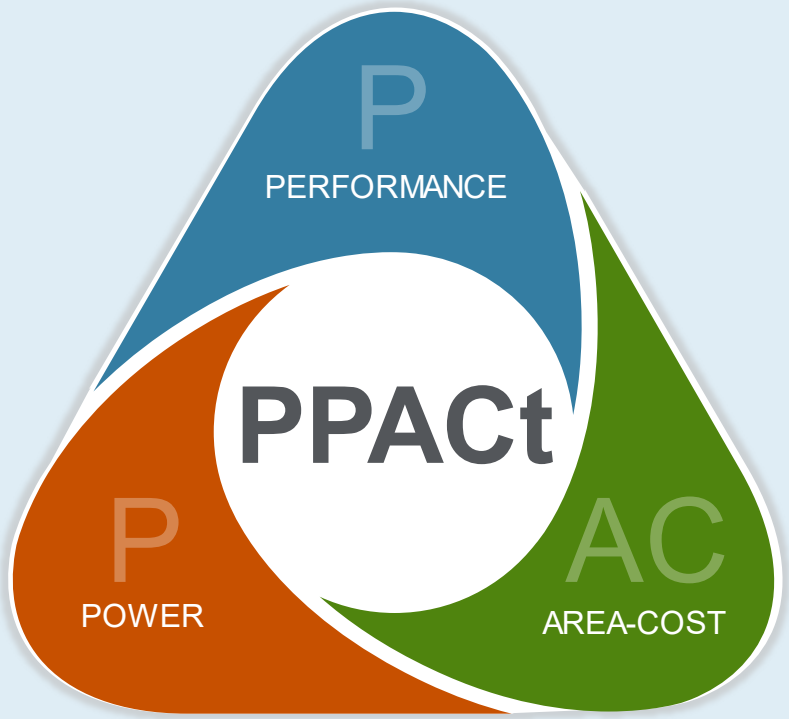
Time to market	▪ Process control ▪ AI^{x}™

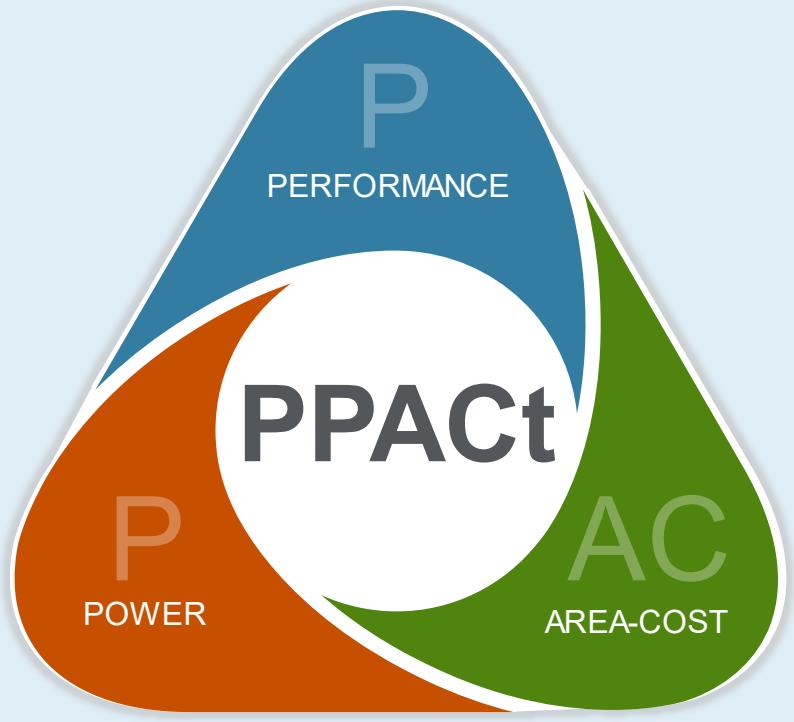
2022 Master Classes

APRIL 21	MAY 26*
New Ways to Shrink	Wiring and Advanced Packaging



* Target date, subject to change

New Playbook for Power, Performance, Area-Cost and Time to Market



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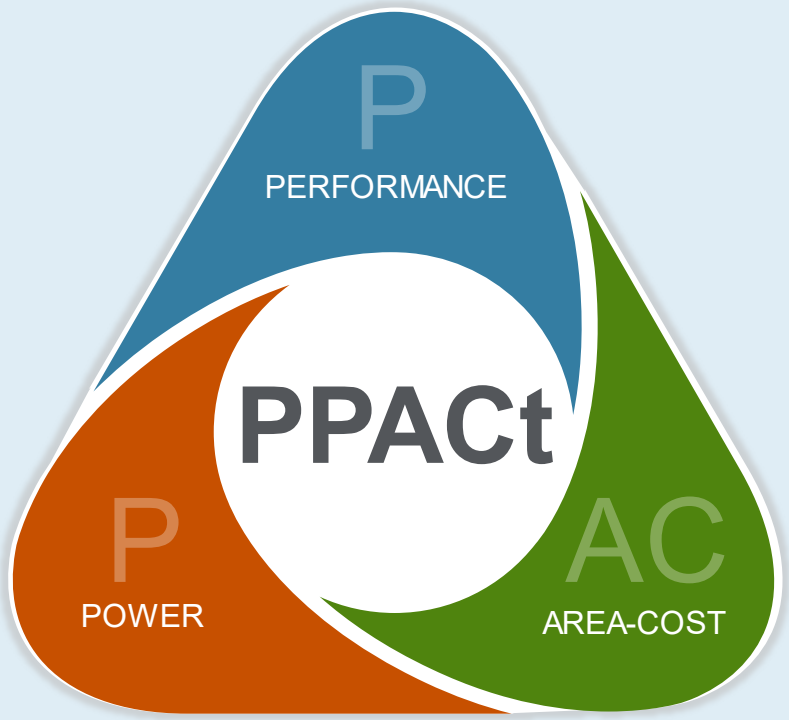
Time to market	▪ Process control ▪ AI^{x}™

2022 Master Classes

APRIL 21	MAY 26*	2H'22
New Ways to Shrink	Wiring and Advanced Packaging	Subscriptions and Services



* Target date, subject to change

AGENDA

9:00	PART 1	**Mike Sullivan** Welcome and Introduction
9:05	PART 2	**Regina Freed** Extending Classic Moore's Law Scaling EUV Enablement with Novel Materials Engineering and AI[X™] **Ofer Adan** 3D Patterning Control Using eBeam Metrology to Solve Edge Placement Errors **Uday Mitra, Ph.D.** Beyond 2D Scaling DTCO with Gate-All-Around and Backside Power Distribution
9:45	PART 3	**Raman Achutharaman, Ph.D.** Growth Opportunities in EUV Enablement, DTCO and GAA
9:55	PART 4	**Q&A** Regina, Ofer, Uday, Raman, Mike

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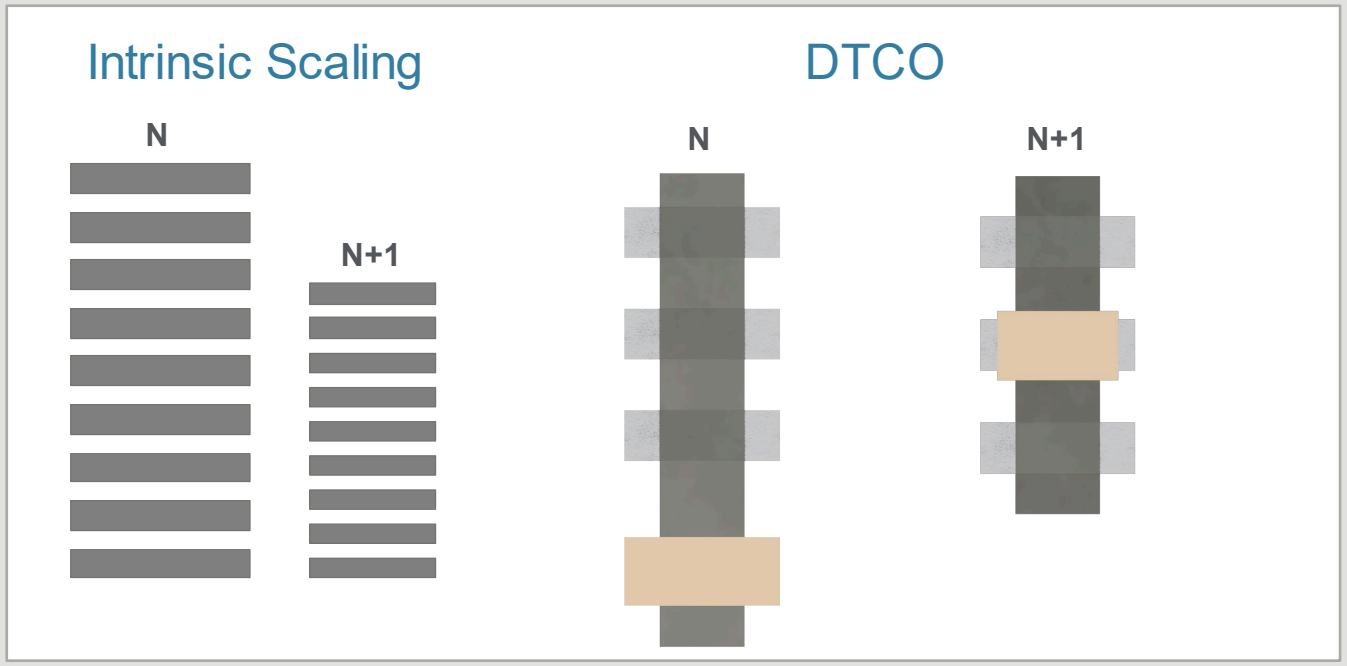
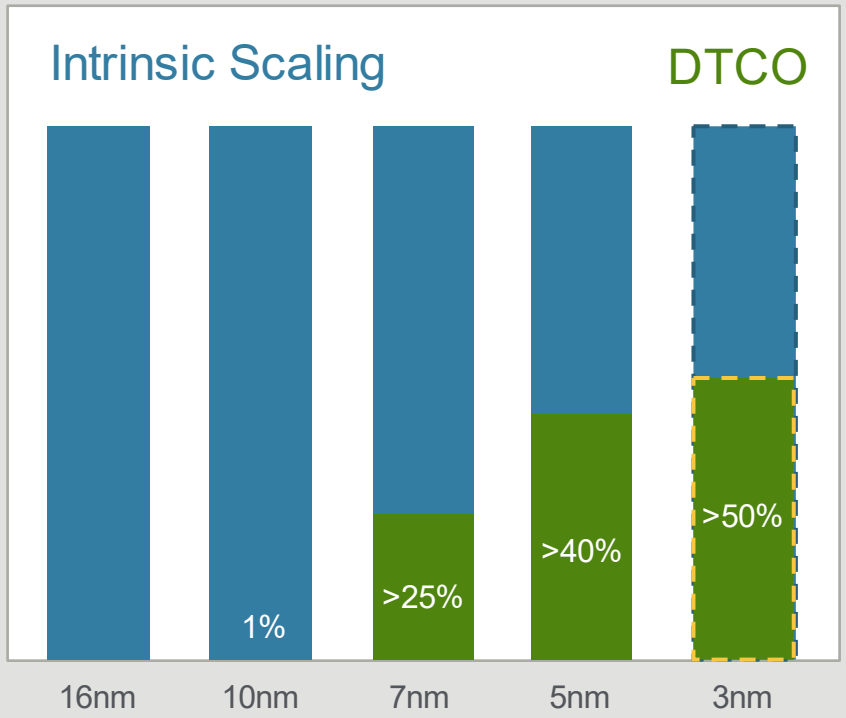
Extending Classic Moore's Law Scaling: EUV Enablement with Novel Materials Engineering and AIx™

Regina Freed
Corporate Vice President
Semiconductor Products Group

NEW WAYS TO SHRINK MASTER CLASS | April 21, 2022

Device Scaling Approaches



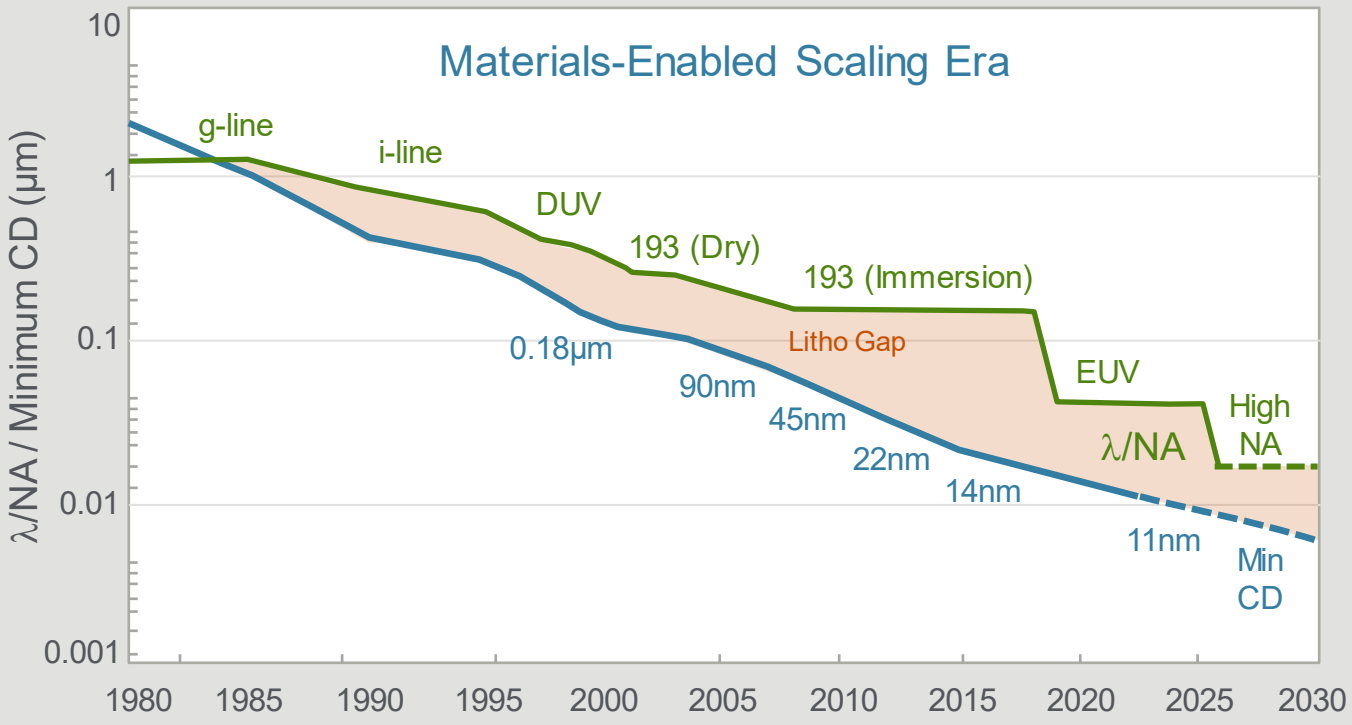


Source: M. Liu/tsmc, ISSCC 2021

DTCO: Design Technology Co-Optimization

DTCO is becoming an increasingly important contributor to scaling

Pitch Scaling Continues



Resolution Limit	K (λ/NA)
193i Litho Etch	80nm
SADP	40nm
SAQP	20nm

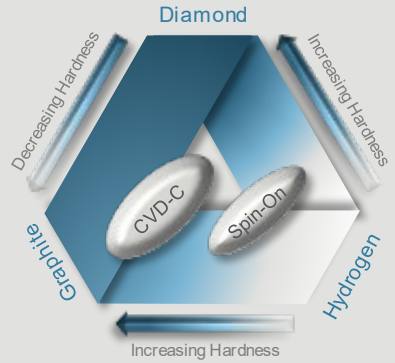
EUV Litho Etch	25nm
SADP	12.5nm
High NA EUV	16nm

CD: Critical Dimension
DUV: Deep Ultraviolet
EUV: Extreme Ultraviolet
NA: Numerical Aperture
SADP: Self-Aligned Double Patterning
SAQP: Self-Aligned Quadruple Patterning

Minimum pitch = lithography capabilities + materials engineering

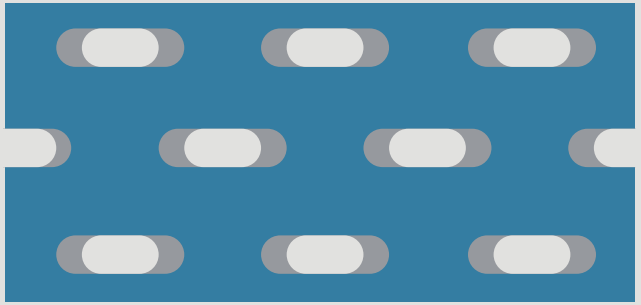
Applied Technologies that Enable EUV Patterning

High-Selectivity CVD Carbon Films

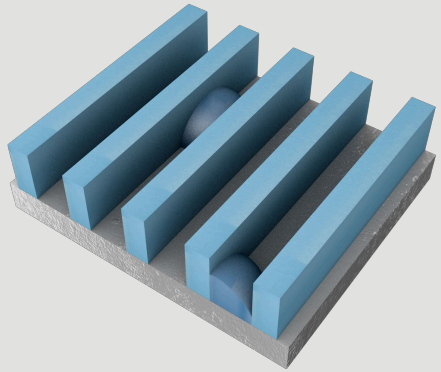


Single-Chamber Etch and Deposition

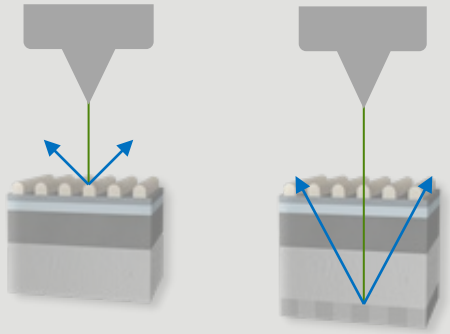
EUV Pattern Extension



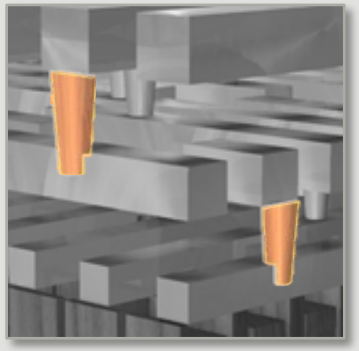
EUV Bridge Removal



eBeam Metrology



3D Edge Placement Control




Deposition

+


Etch

+


Metrology

+

=

AI^{x} to accelerate R&D and widen process windows

CVD: Chemical Vapor Deposition
eBeam: Electron Beam

ADI: After Develop Inspection
AEI: After Etch Inspection
AI^{x}: Actionable Insights™

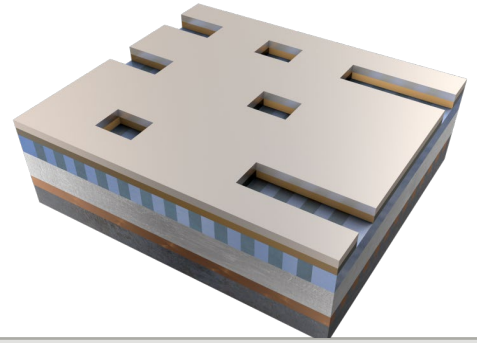
Creating Patterns with EUV Lithography

LINES / GRATING

Create main pattern

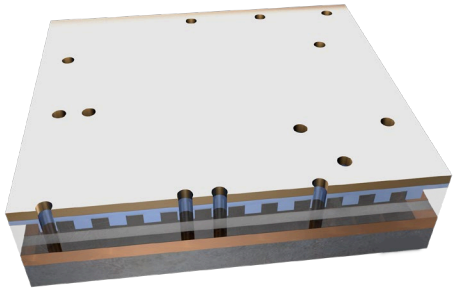
CUTS

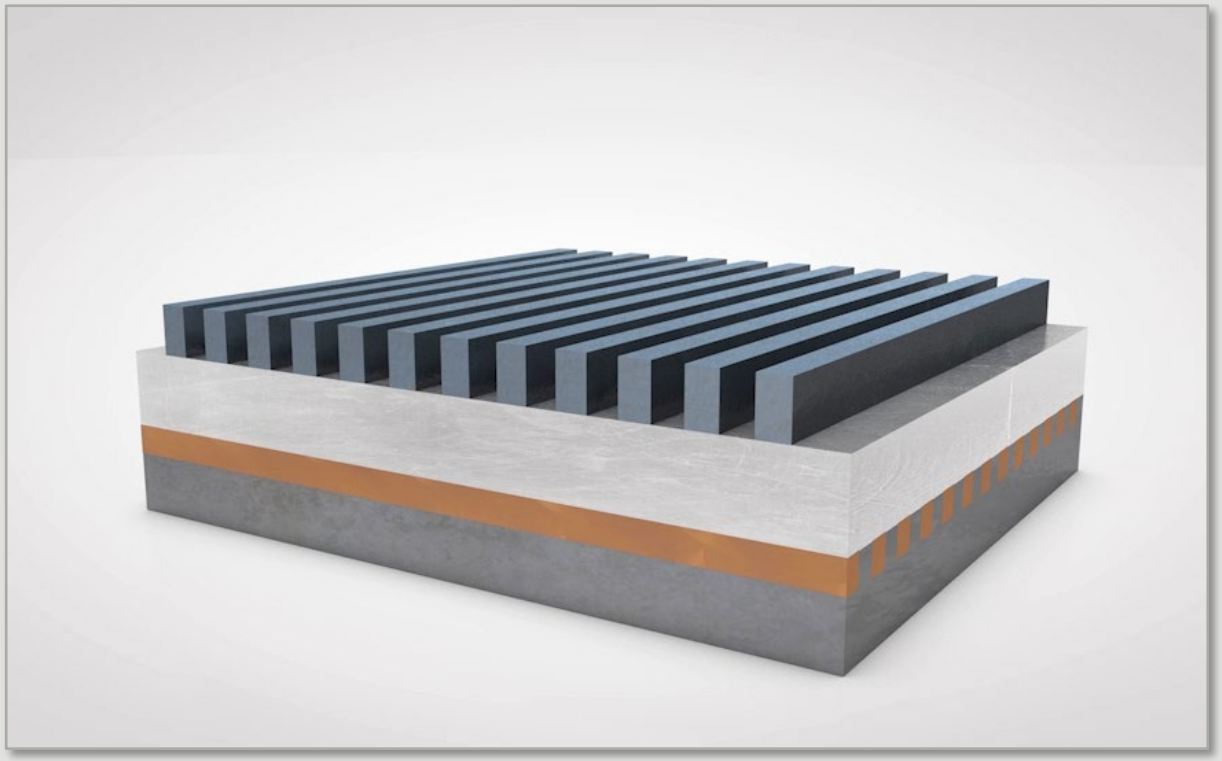
Segment lines



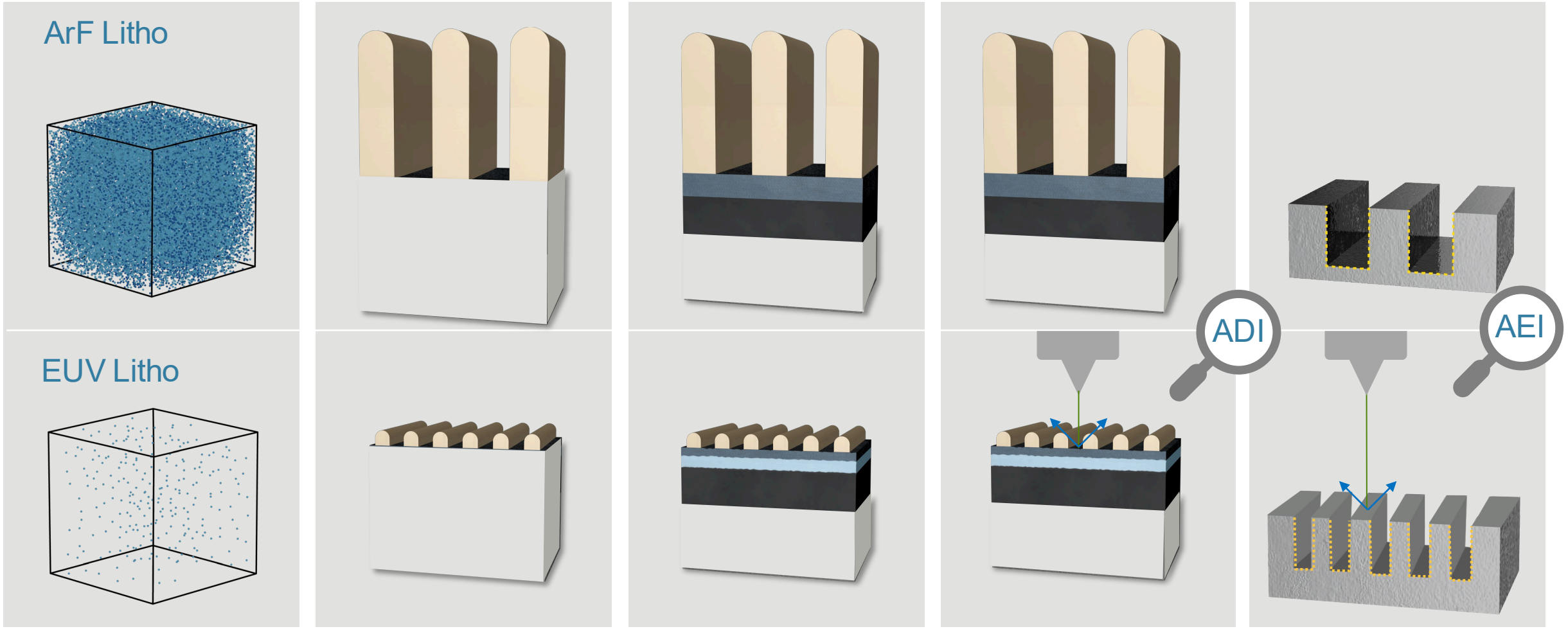
VIAS

Connect levels





Patterning Control Challenges in EUV Lithography



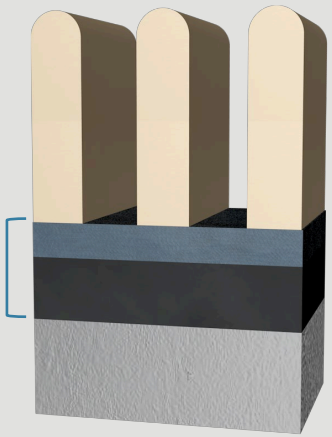
Source: M. Smith et al., Proc of SPIE, 2009

>10X fewer photons	Thinner resist	Transfer layer, hardmask variability	Small features, resist sensitivity	Smaller features

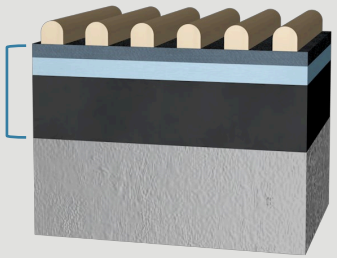
ArF: Argon Fluoride

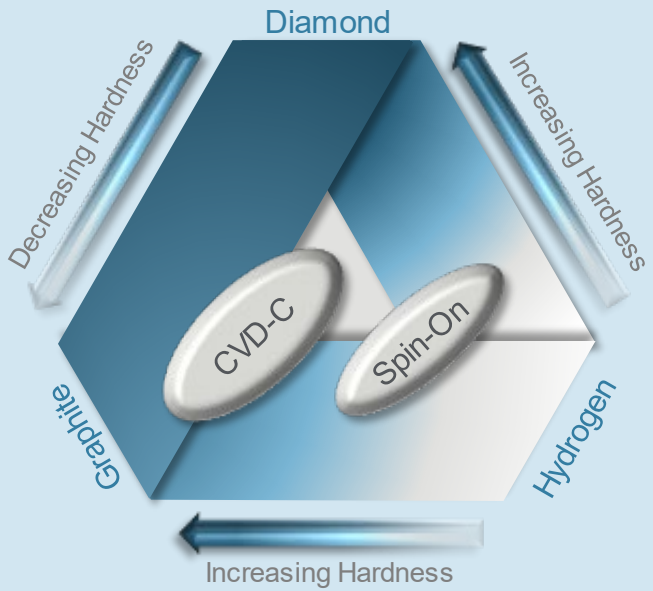
New CVD Carbon Films for EUV Pattern Transfer

ArF Litho



EUV Litho





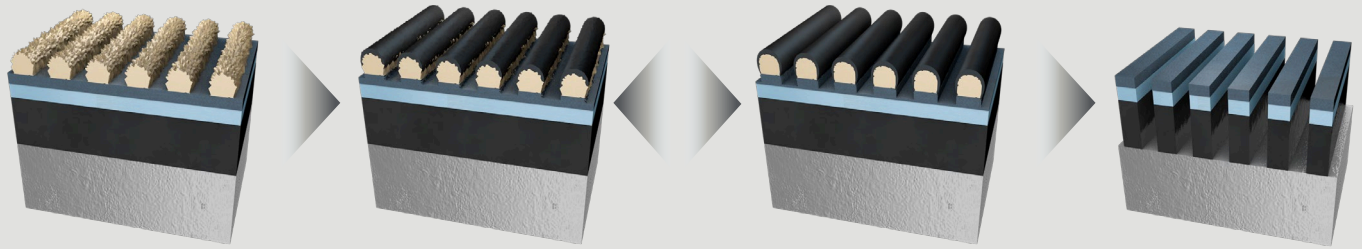
Applied Precision Stensar™ Advanced Patterning Film

- Dense, high-selectivity layers
- Tunable stress for line variability control
- Film stack interface control improves yields
- Low defectivity

Adapted from: J. Robertson, Mat Sci and Eng., 2002

CVD: Chemical Vapor Deposition

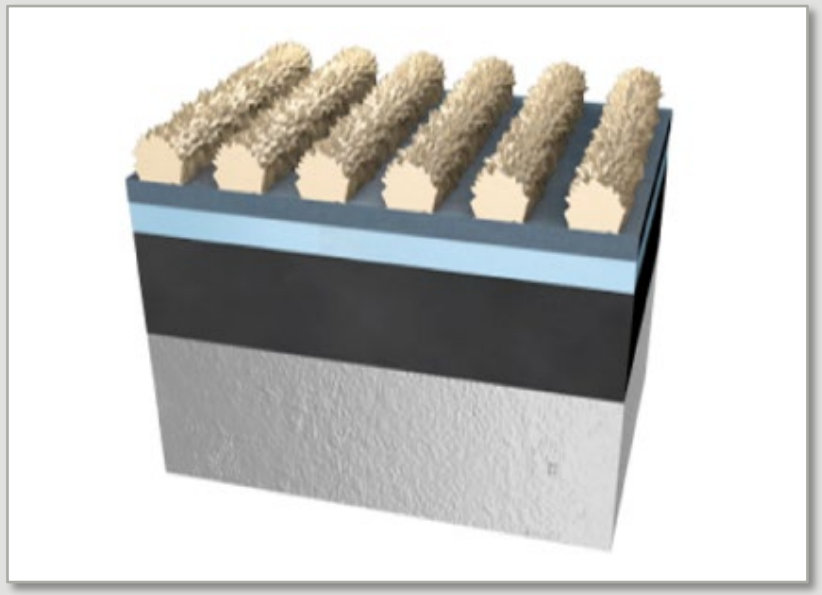
Innovative Etch Technology Corrects Stochastic Errors

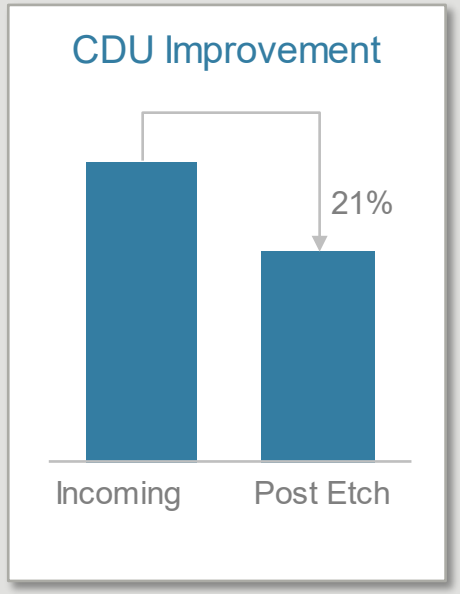


Rough EUV photoresist

Single-chamber etch + dep technique improves EUV photoresist patterns

Improved patterns





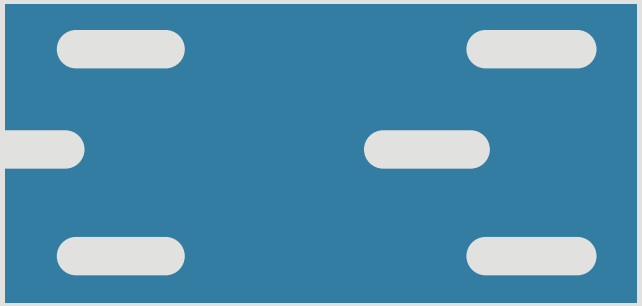
Applied Centris® Sym3® Y Etch

- Alternate between deposition and etch in the same chamber
- Extensive pulsing modes shape photoresist profile
- Symmetry of gas flow, plasma and wafer temperature produces uniform results across the wafer
- High conductance quickly removes by-products

CDU: Critical Dimension Uniformity

Directional Patterning Technology

EUV 1
First half of desired pattern



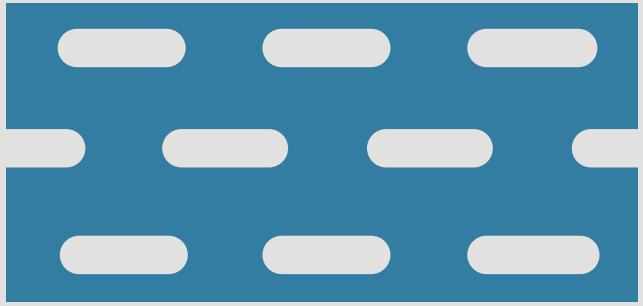
Top View

+

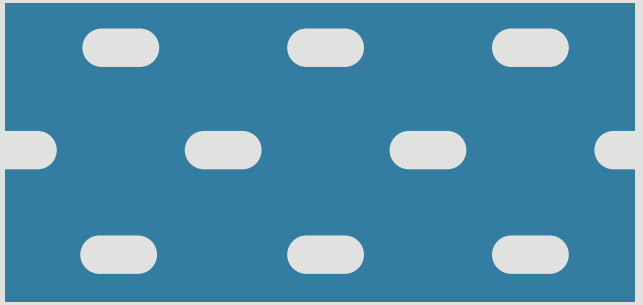
EUV 2
Second half of desired pattern

=

Final Pattern



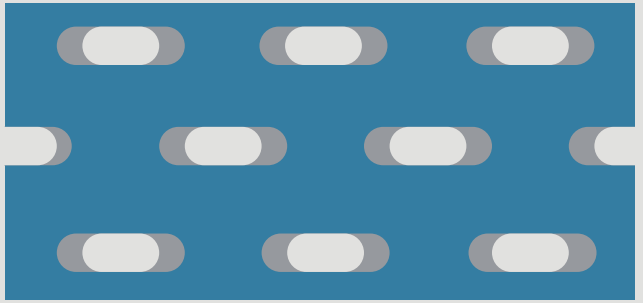
EUV
All vias patterned at minimum EUV spacing



Top View

+

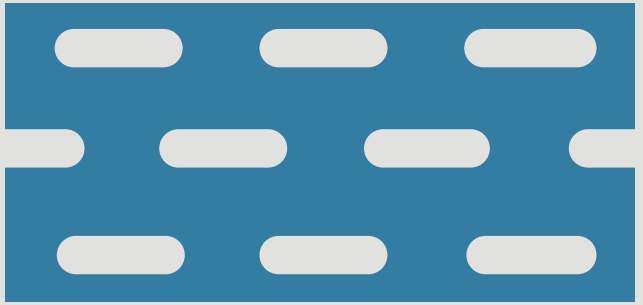
EUV Patterns Extended



Side View

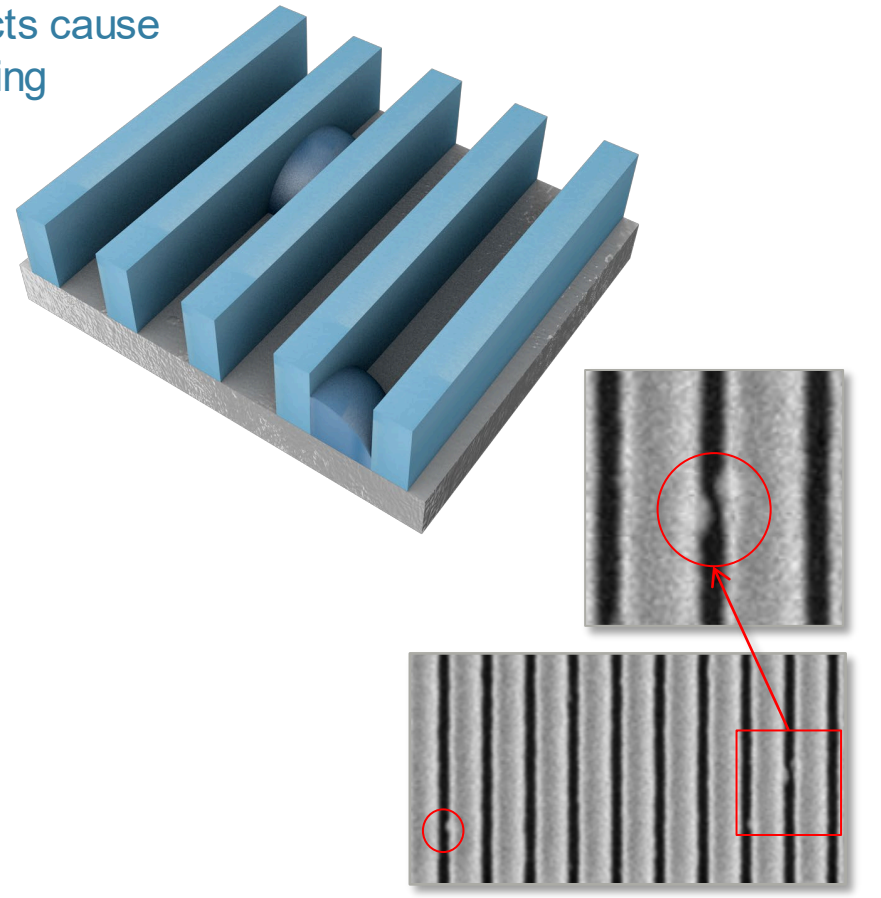
=

Final Pattern

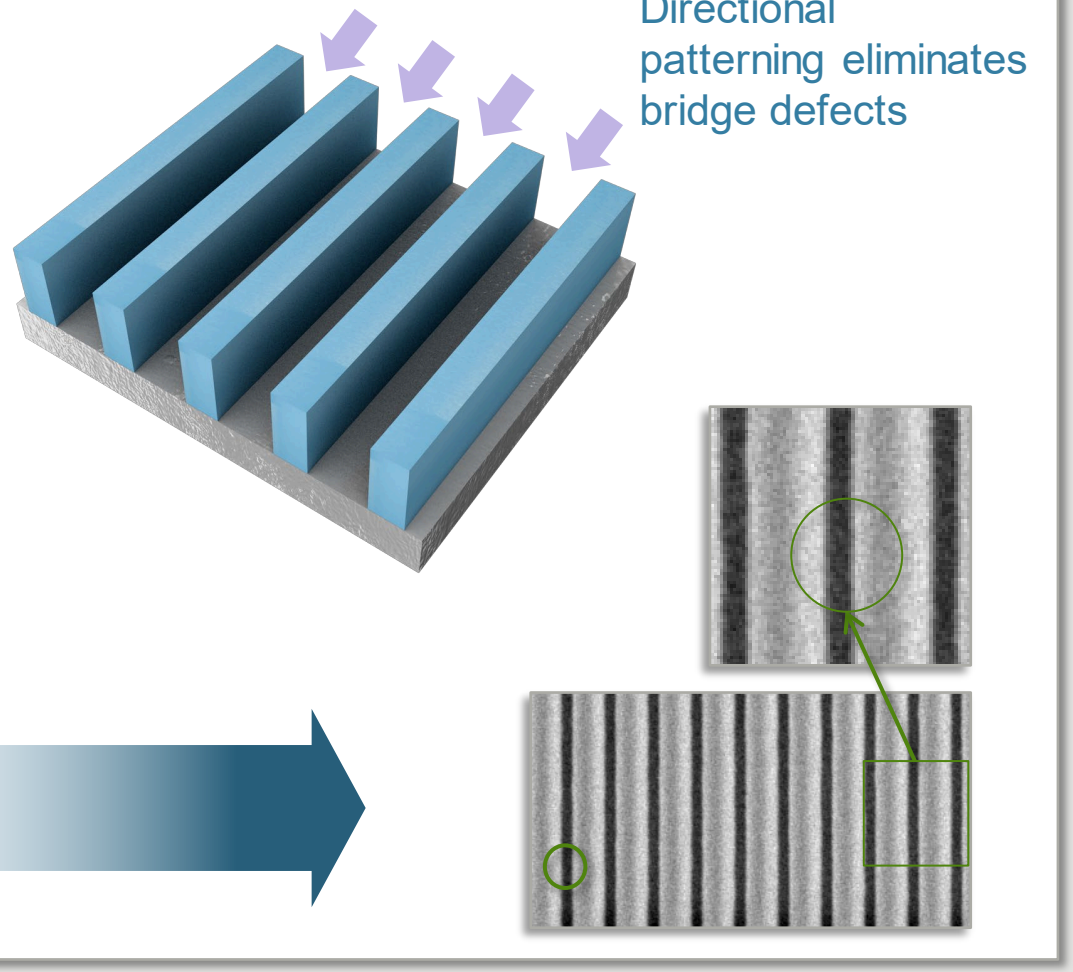


Directional Patterning: Stochastic Defect Removal

EUV stochastic defects cause bridging



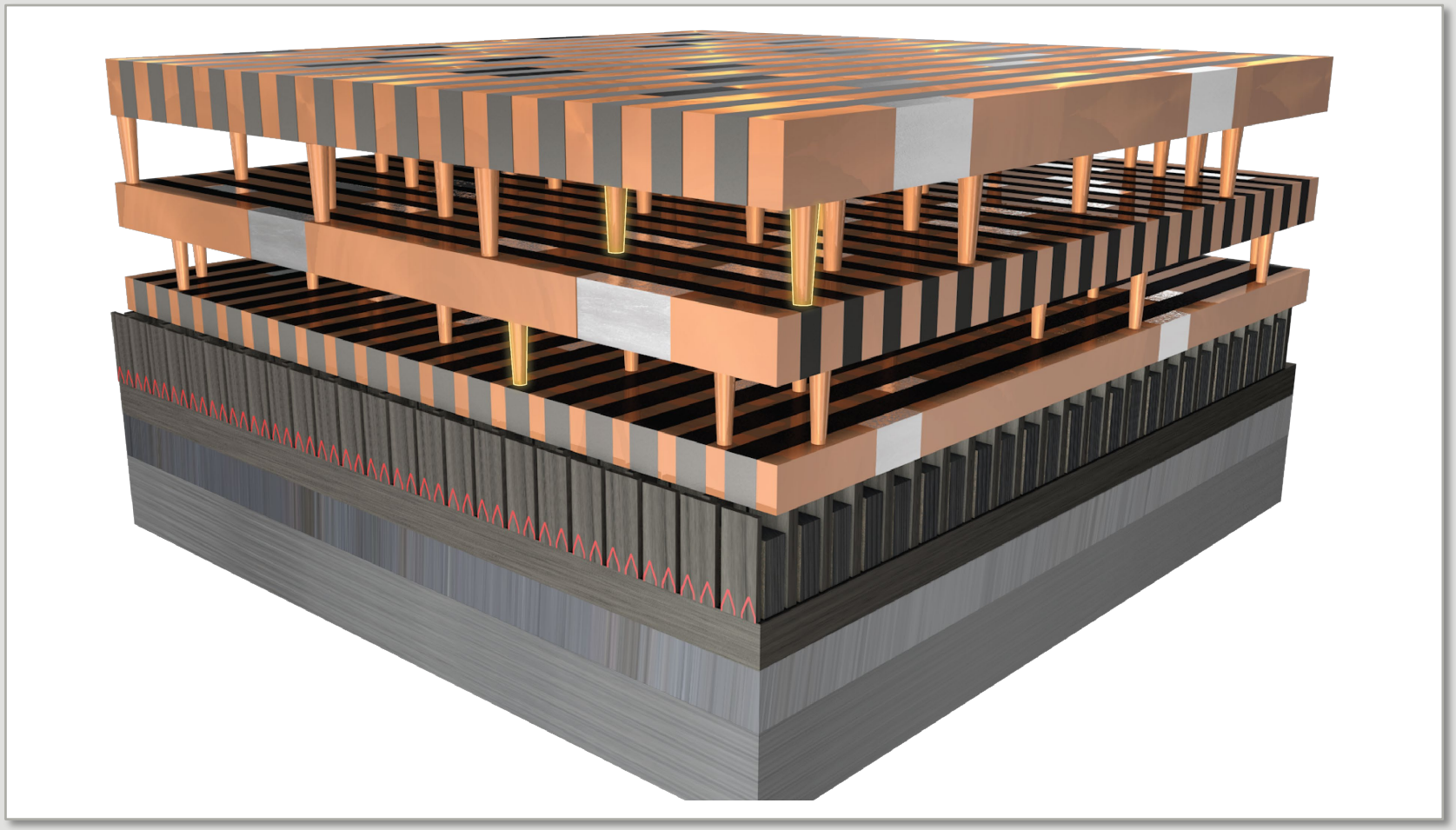
Directional patterning eliminates bridge defects



Source: Applied Materials

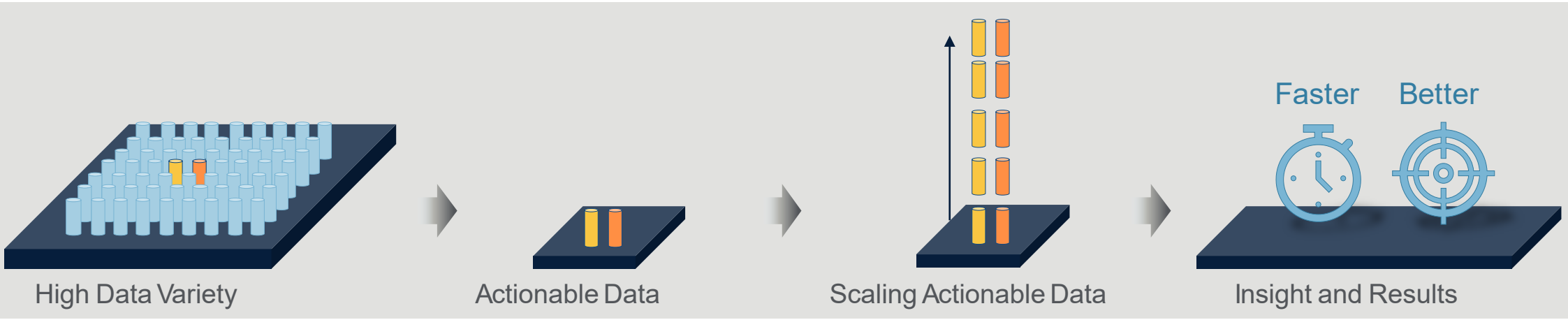
RIE: Reactive Ion Etch

Edge Placement: A Growing Challenge



3D metrology needed to overcome stochastic errors and process variability

Actionable Insights (AI^{x}) Accelerate Time to Solution



Proprietary Sensors

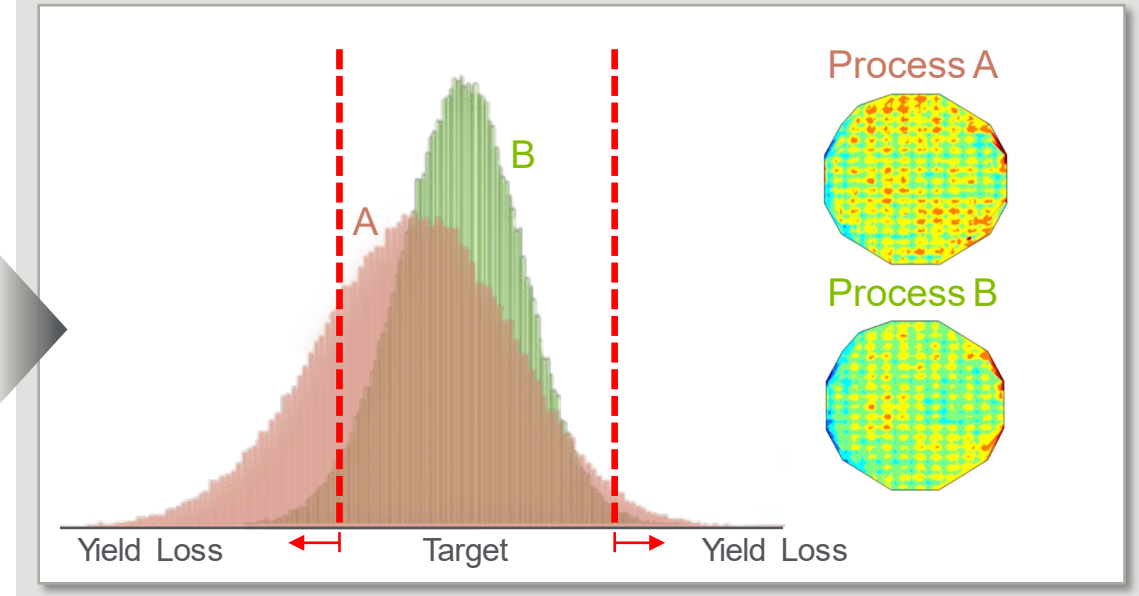

Deposition


Etch

Custom Metrology


Metrology

AI^{x} Analytics Platform



3D Patterning Control Using eBeam Metrology to Solve Edge Placement Errors

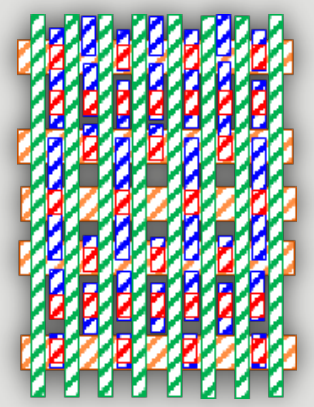
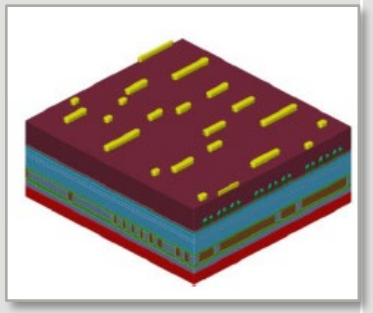
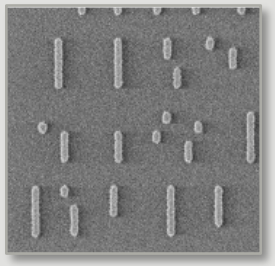
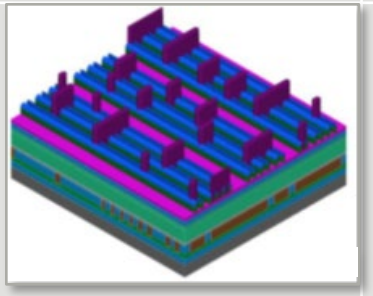
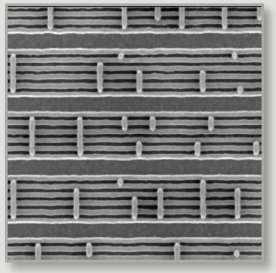
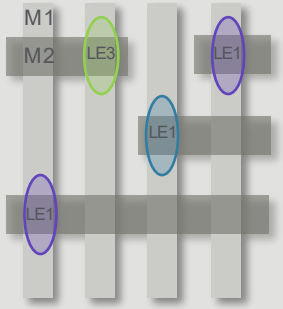
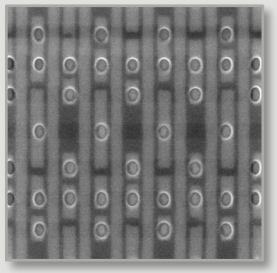
Ofer Adan

Senior Director

Process Diagnostics and Control Group

NEW WAYS TO SHRINK MASTER CLASS | April 21, 2022

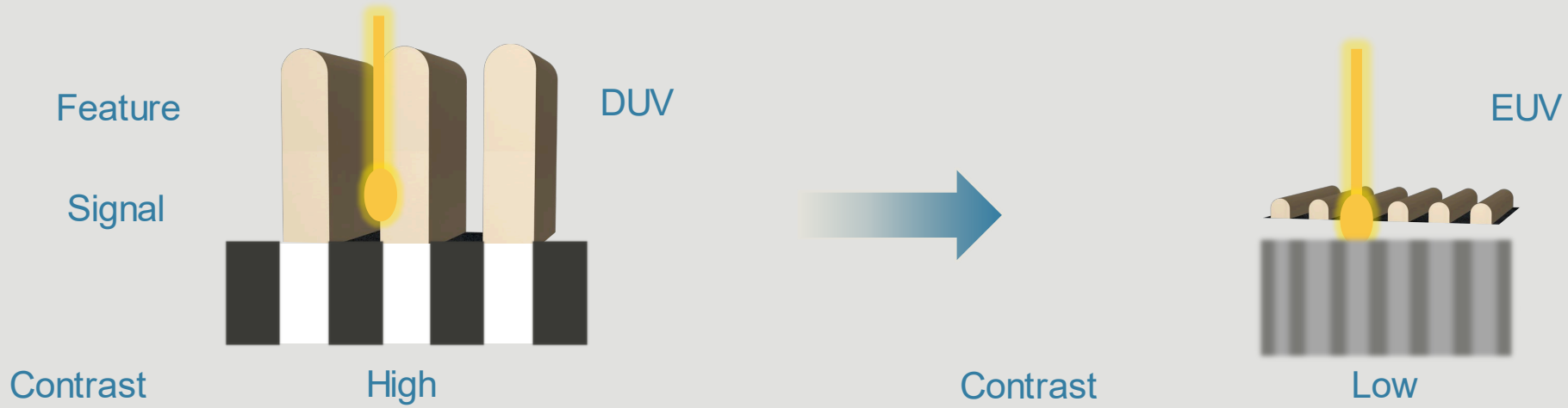
Patterning Control Metrology Overview

Chip Design	Goals		Measurements	Tools	eBeam Images
 CAD Layout	1. Pattern for each layer correctly transferred to resist		ADI: Pattern centering CD uniformity	Optical overlay VeritySEM® PROVision®	
	2. Pattern on resist correctly etched into wafer		AEI: Correlation with ADI	VeritySEM PROVision	
	3. Edges of features in adjacent layers correctly aligned		3D patterning control	PROVision	

Source: imec/Applied Materials: "Minimizing EUV Edge Placement Error by Fast High-Resolution SEM"

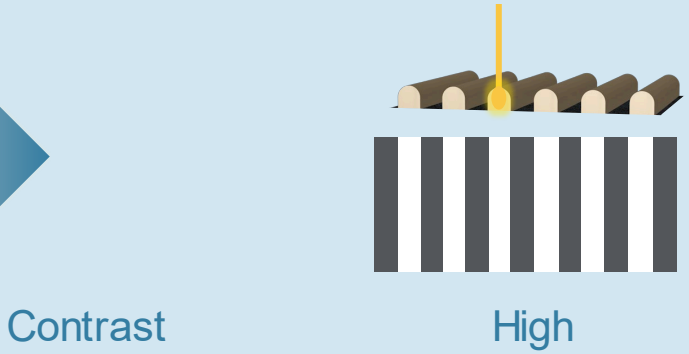
EUV ADI Needs Lower eBeam Energy, Higher Pattern Resolution

Challenge



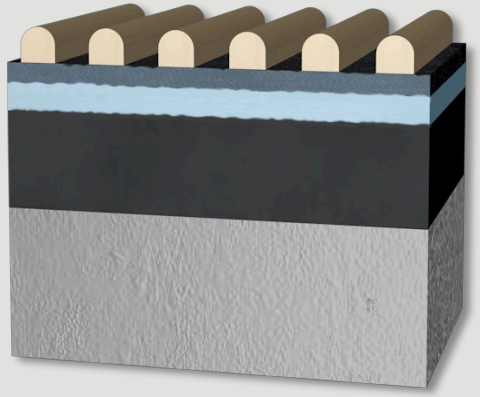
Upcoming VeritySEM System

High Resolution at Low Energy

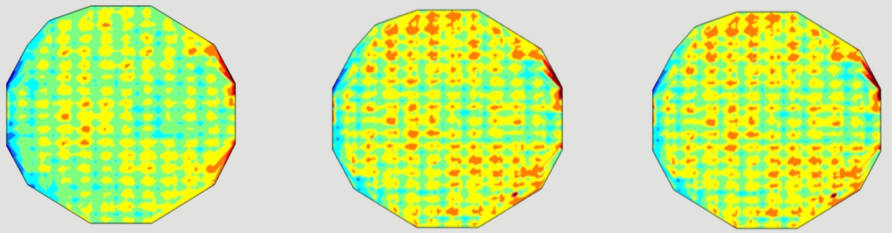


Pattern Fidelity from Development to Etch

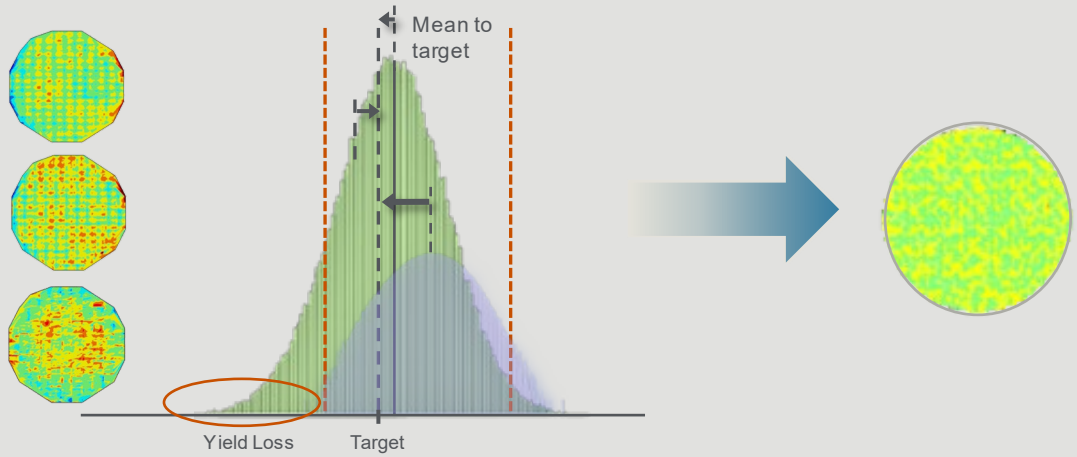
EUV Patterning Stack



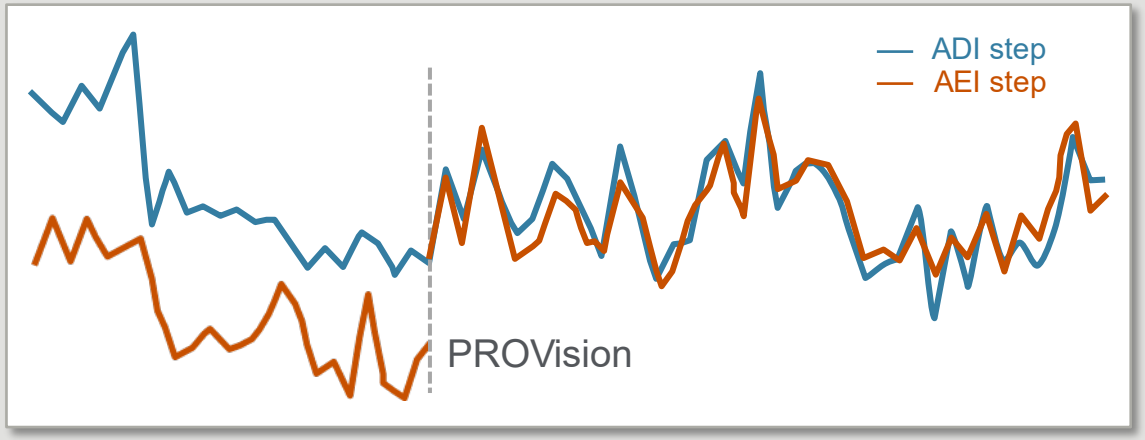
Sources of Variability



Multilayer CDU Metrology

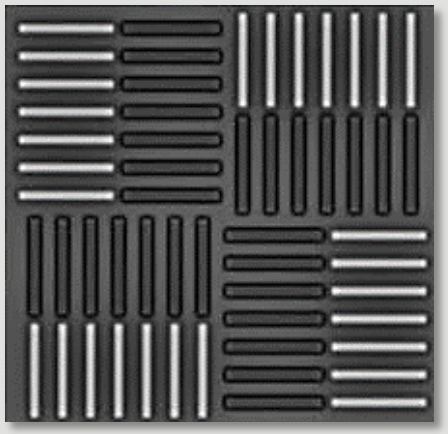


Higher ADI-AEI Correlation

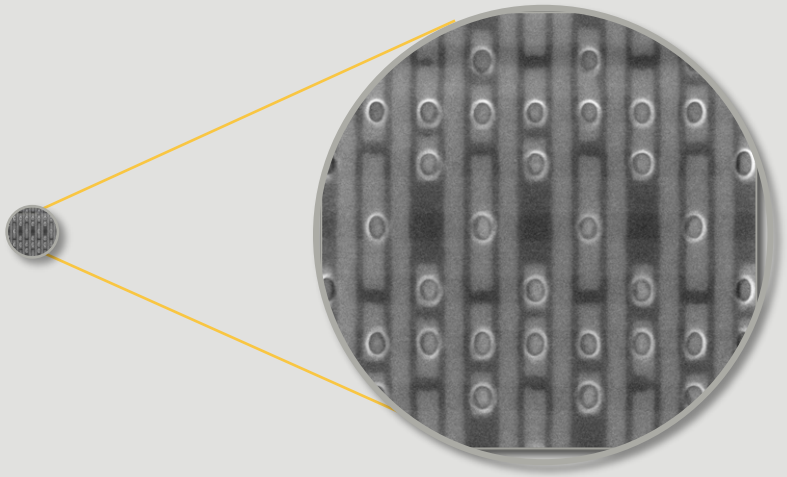


Source: Cornel Bozdog, Micron Technology, Inc. (United States) "Metrology Requirements Driven by Memory Scaling" (Keynote Presentation) Paper 11325-100, AEI mentioned as ACI in the source.

EUV Device Features >10X Smaller than Optical Overlay Targets



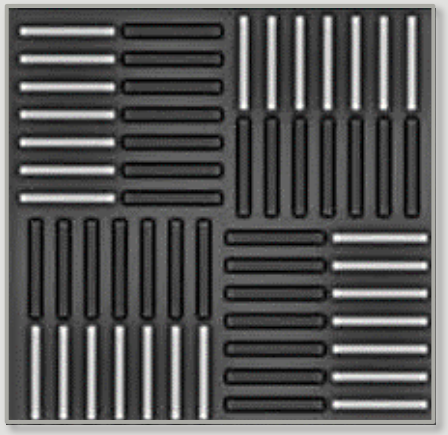
Optical Proxy Target



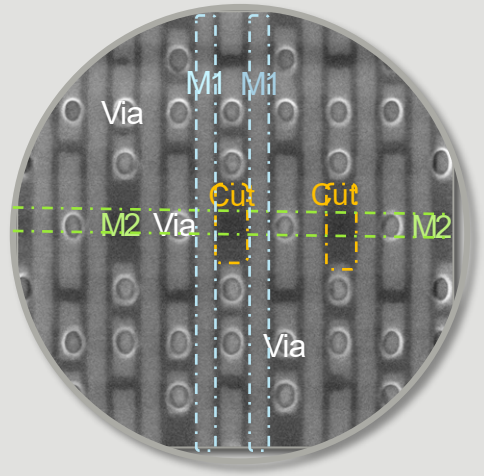
On-Die Features

Source: EUV+SADP Applied Materials and IMEC

Element 1: On-Device Metrology



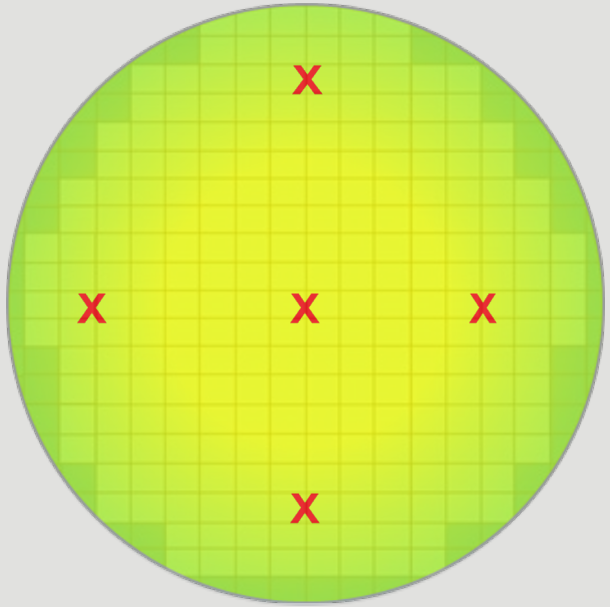
Optical Proxy Target Approximation



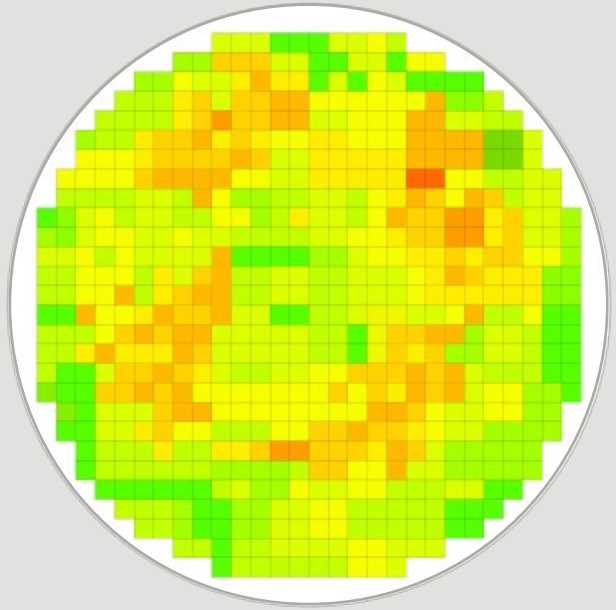
On-Device eBeam Metrology

Source: EUV+SADP Applied Materials and IMEC

Element 2: Massive Across-Wafer Metrology

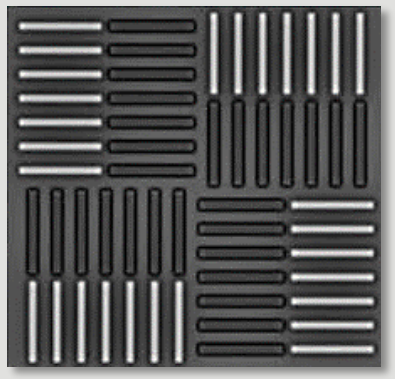


Statistical Sampling



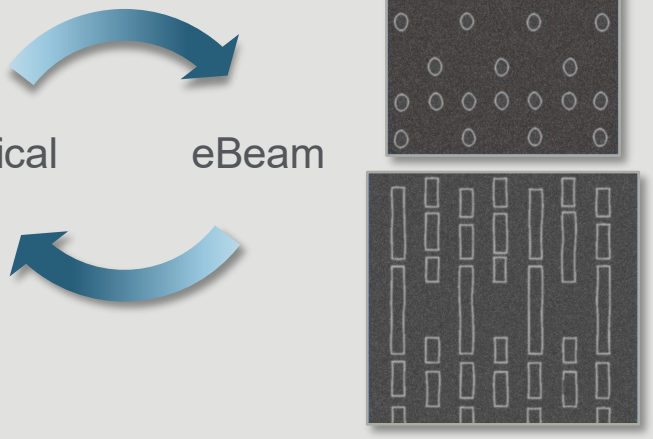
Massive Measurements

Element 3: 3D Integrative Metrology

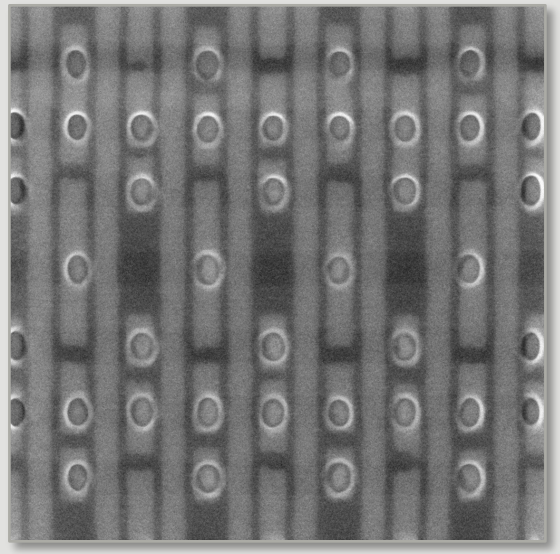


Optical Proxy Target
Approximation

Source: Applied Materials



2D One Layer at a Time
Low-Energy Multibeam
Feedback to Scanner



3D Multilayer
High-Energy PROVision
Feedback to all EPE Sources

Source: EUV+SADP Applied Materials and IMEC

Applied PROVision 3E eBeam Metrology System

Edge Placement Error (EPE)

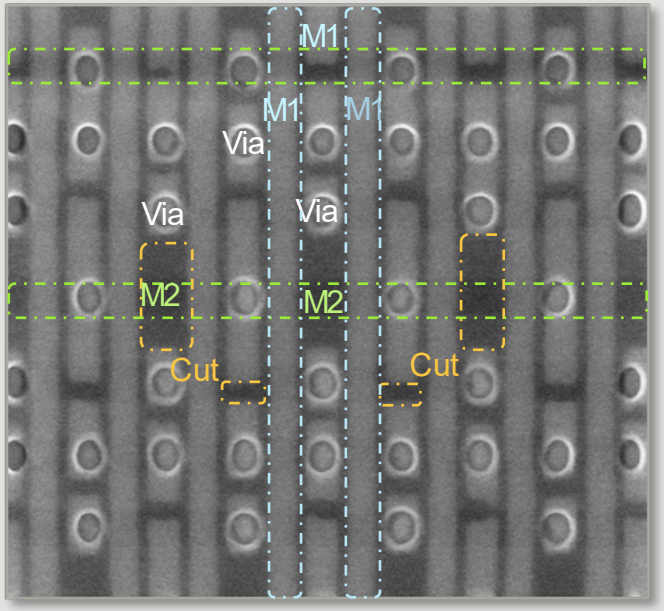


Image Source: Applied Materials

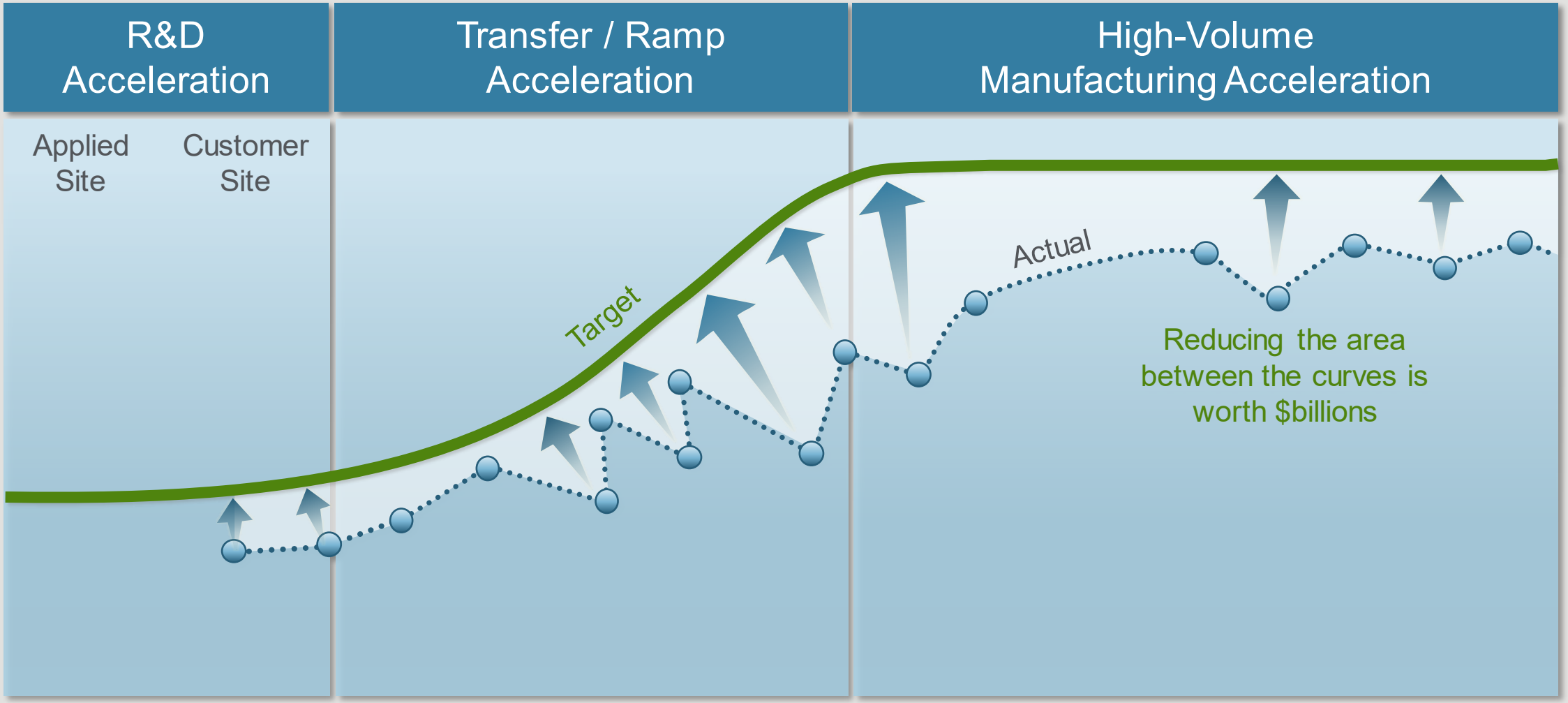
ERROR SOURCES

- Overlay/alignment
- CD uniformity of lines
- CD uniformity of cuts
- Line roughness
- Pitch walking

$$\text{EPE error} = \sqrt{(\Delta\text{overlay})^2 + (\Delta\text{CDU}_{\text{lines}})^2 + (\Delta\text{CDU}_{\text{cuts}}) + (\Delta\text{LWR}_{\text{lines}})^2 + (\Delta\text{LWR}_{\text{cuts}})^2}$$

Equation Source: Paper 9422-61 SPIE 2015 ASML

eBeam Technology Helps Accelerate the “t” in PPACt



Source: Applied Materials

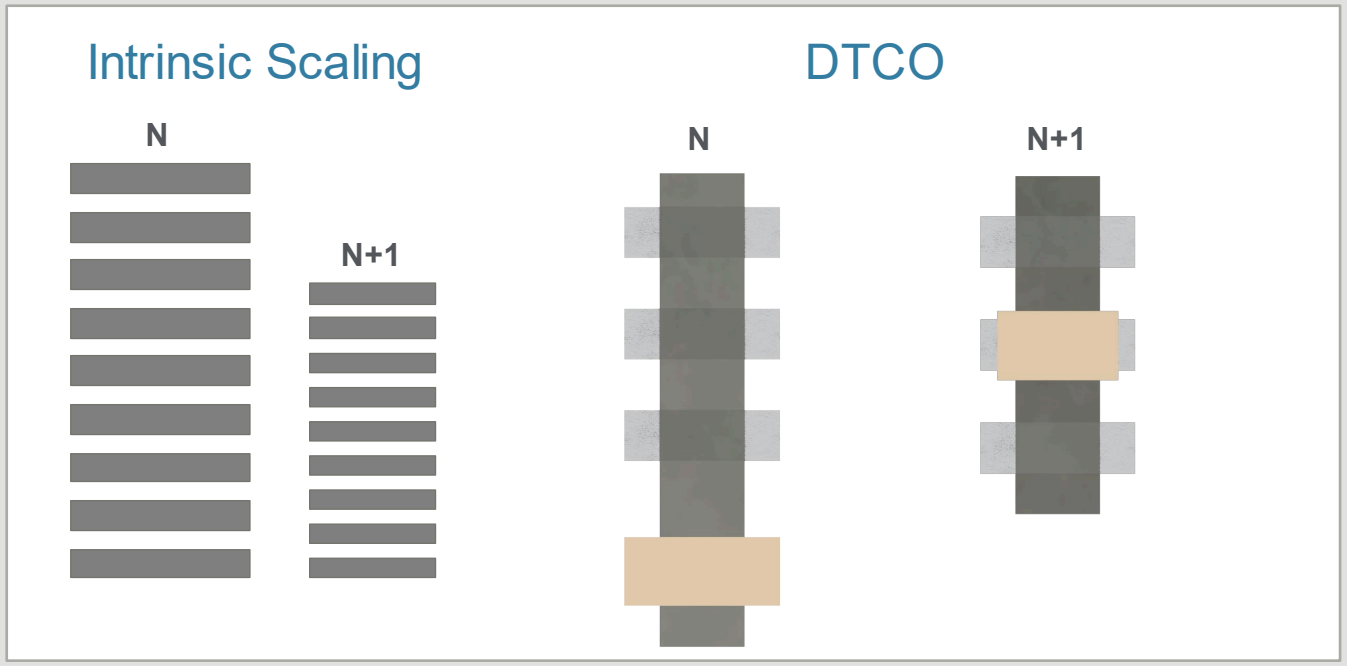
APPLIED MATERIALS®
make possible

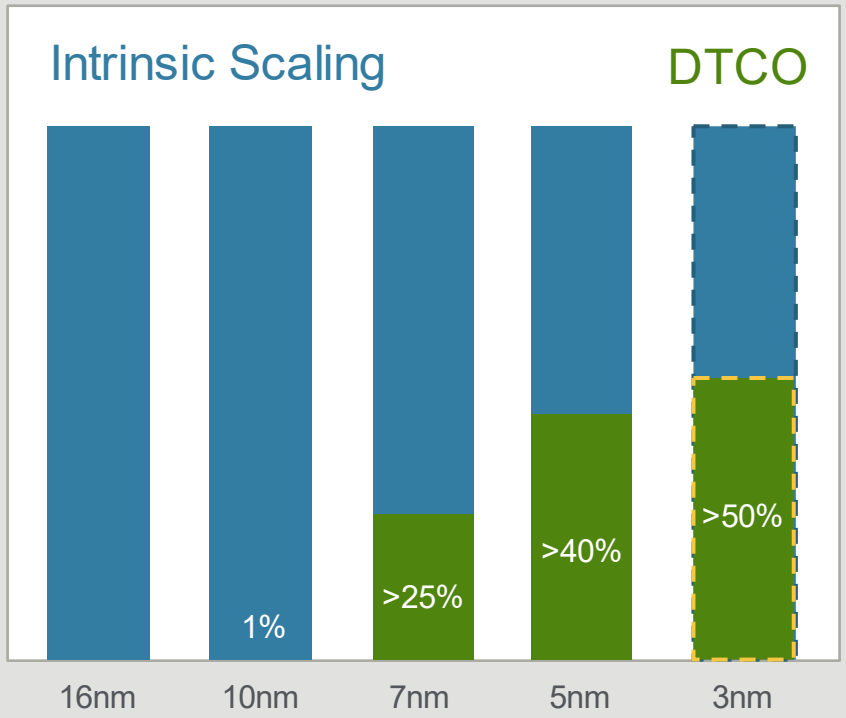
Beyond 2D Scaling: DTCO with Gate-All-Around Transistors and Backside Power Distribution

Uday Mitra, Ph.D.
Vice President
Semiconductor Products Group

NEW WAYS TO SHRINK MASTER CLASS | April 21, 2022

Device Scaling Approaches

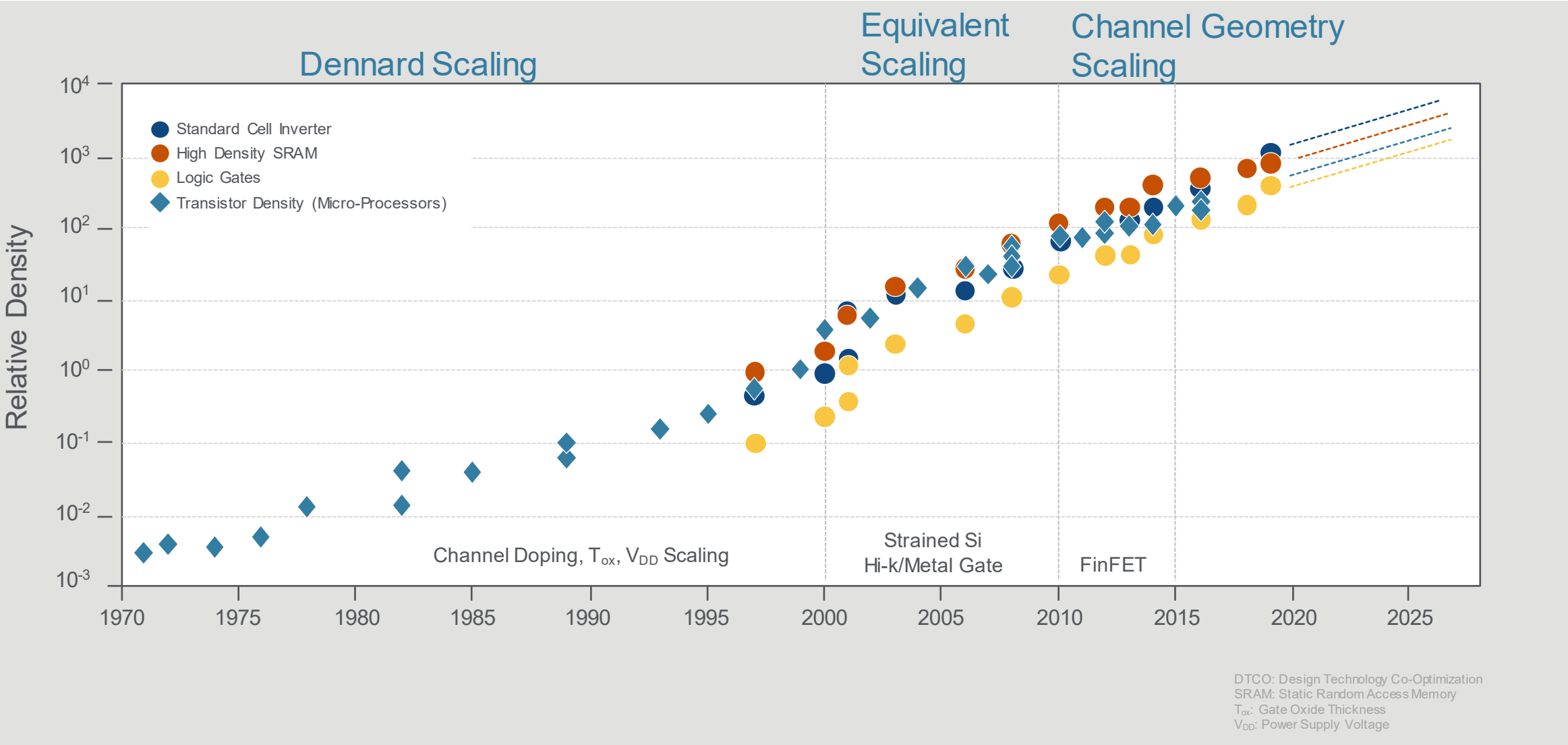




Source: M. Liu/tsmc, ISSCC 2021

DTCO: Design Technology Co-Optimization

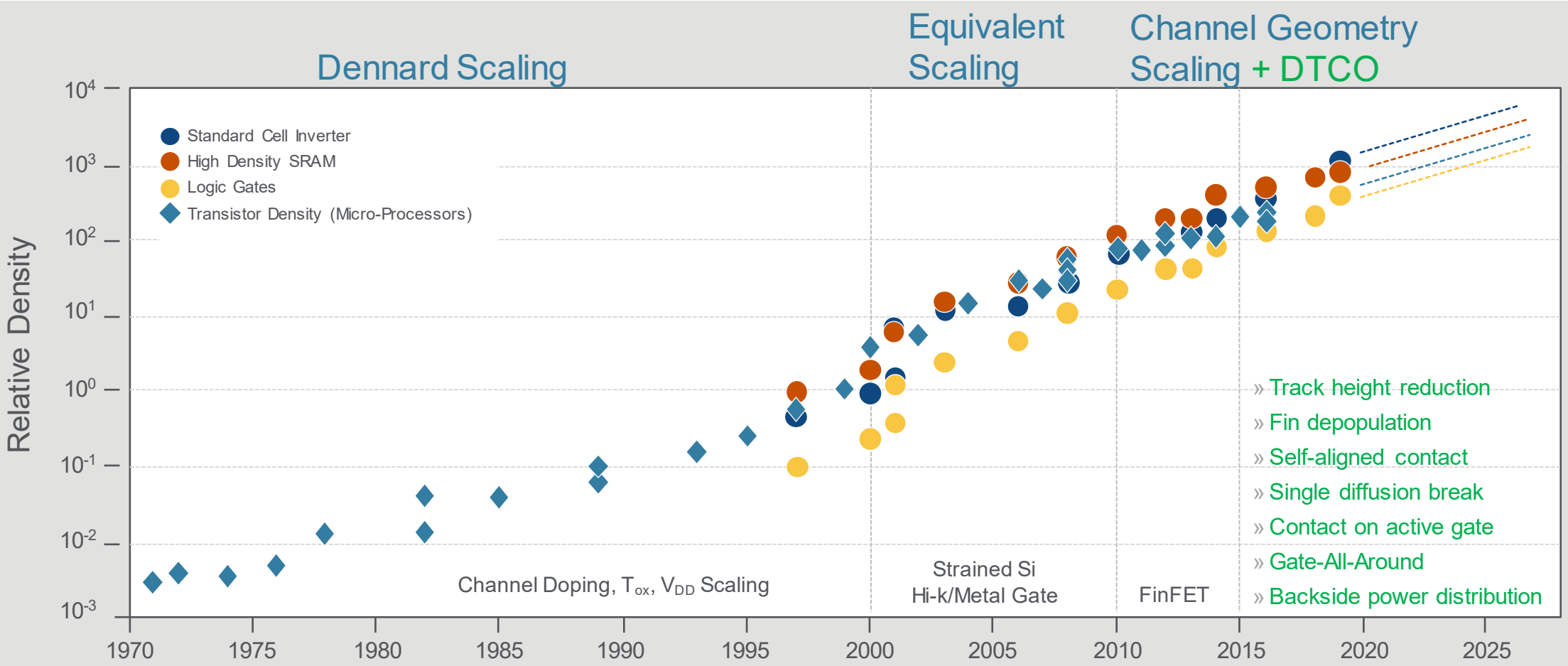
DTCO is becoming an increasingly important contributor to scaling



DTCO: Design Technology Co-Optimization
SRAM: Static Random Access Memory
T_{ox}: Gate Oxide Thickness
V_{DD}: Power Supply Voltage

Source: Jin Cai, TSMC, 2019 IEDM and Applied Projections

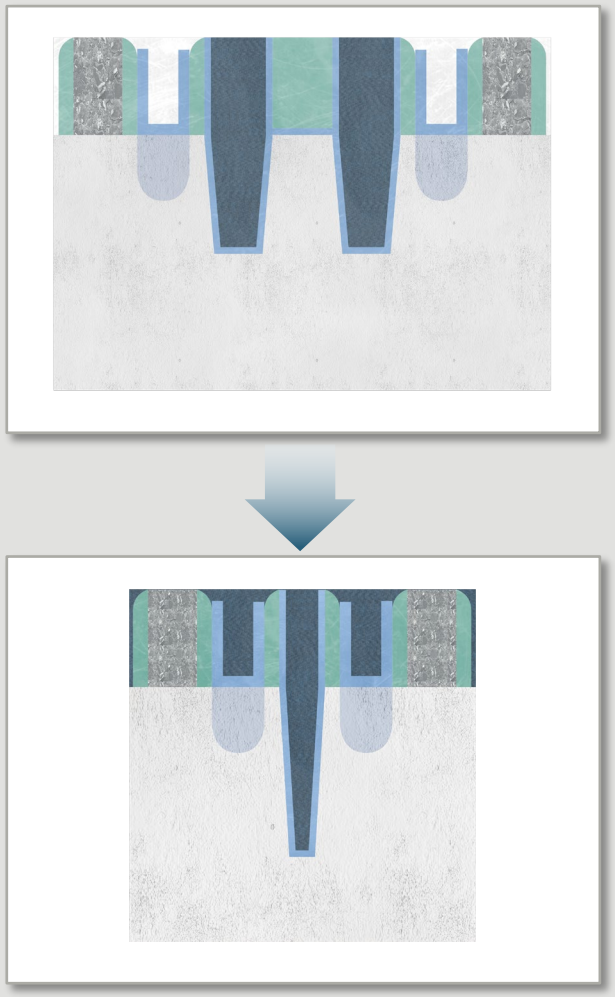
Logic Scaling Continues with DTCO Innovations



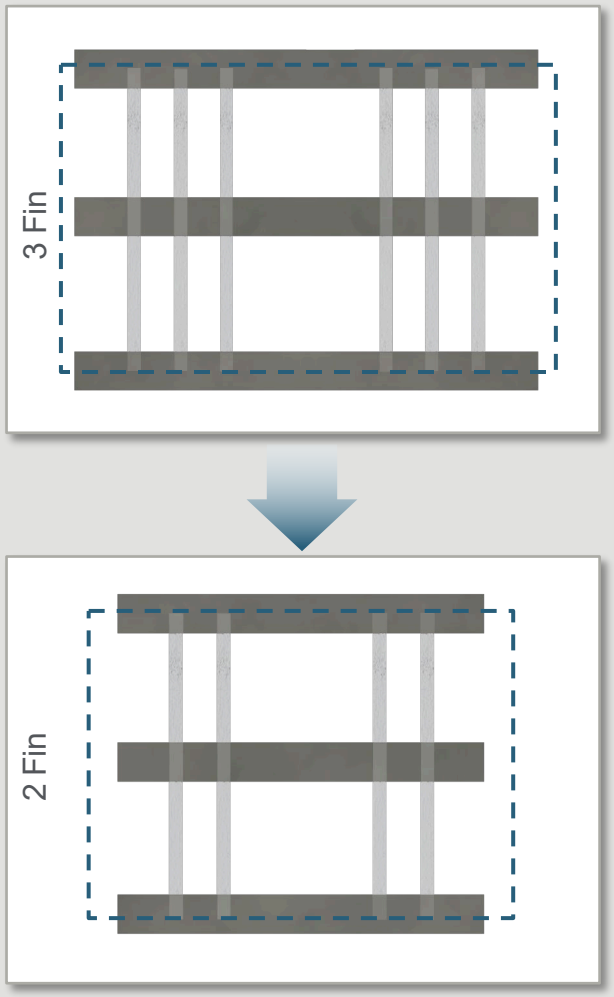
DTCO: Design Technology Co-Optimization
SRAM: Static Random Access Memory
T_{ox}: Gate Oxide Thickness
V_{DD}: Power Supply Voltage

Source: Jin Cai, TSMC, 2019 IEDM and Applied Projections

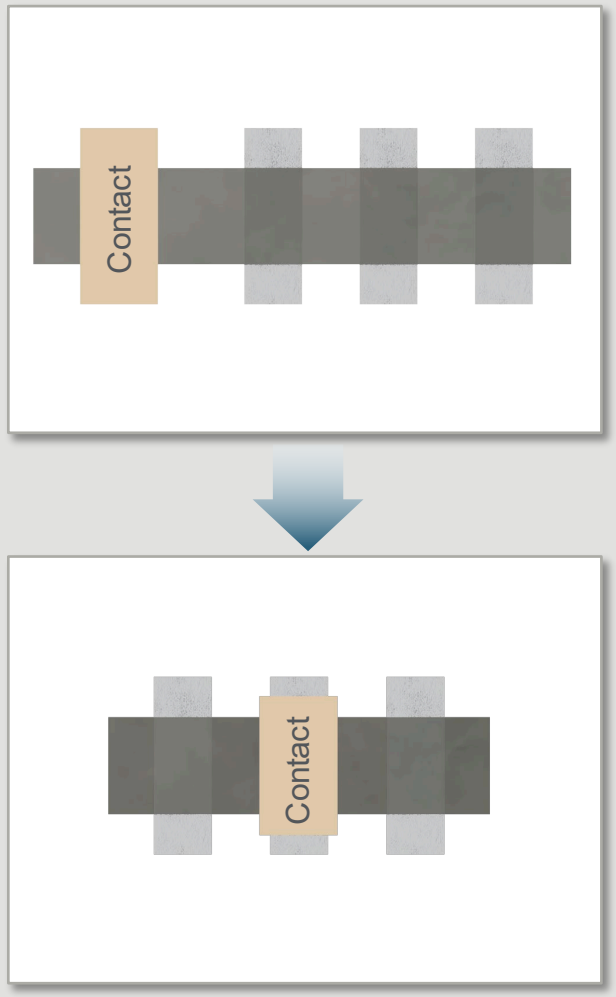
Cell Area Reduction Through DTCO



Single diffusion break



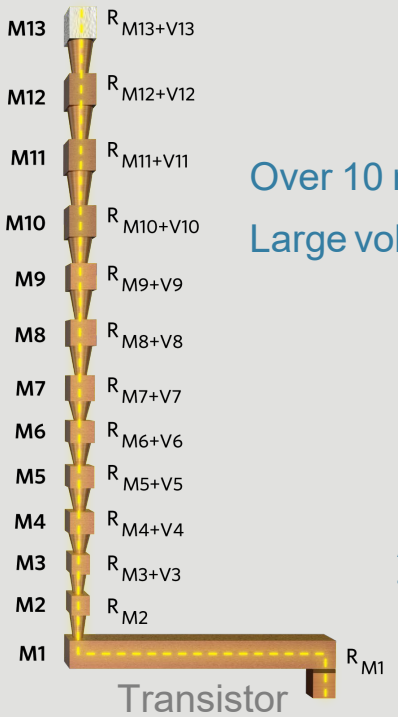
Fin depopulation



Contact over gate

DTCO with Backside Power Distribution Network

Frontside power in

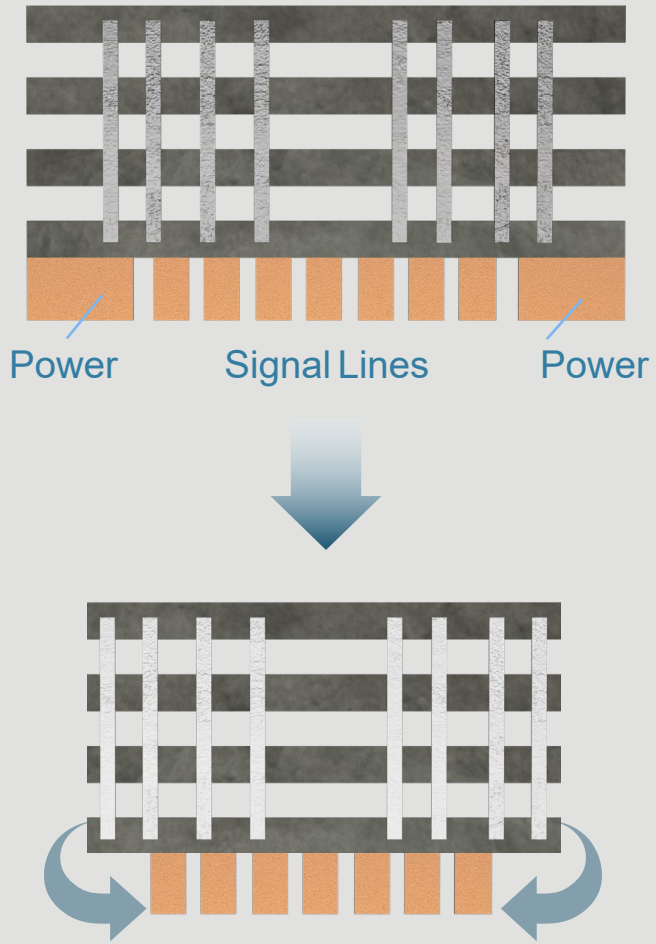


Over 10 metal layers

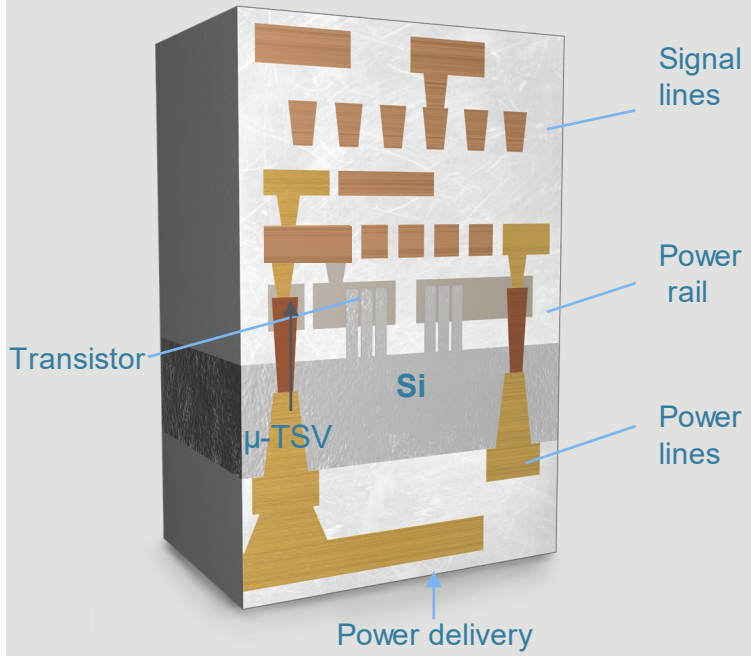
Large voltage drop

Area consumed for power delivery

Power losses and area penalty



Power lines moved below



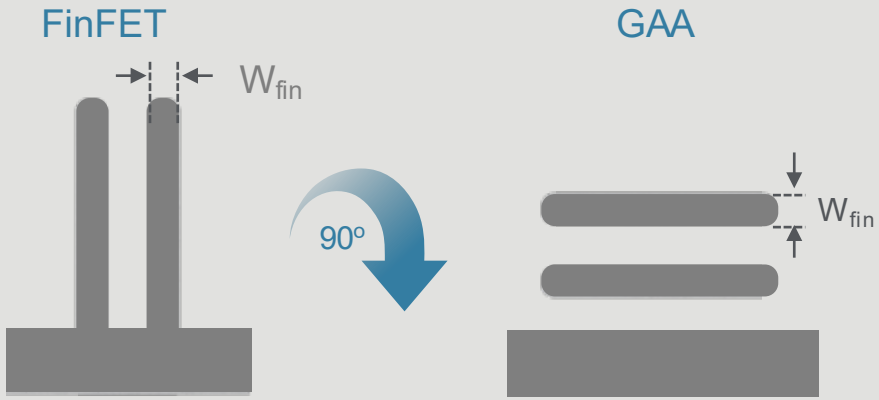
Reduces power from 3-25%[1]

Increases logic density from 6-30%[1]

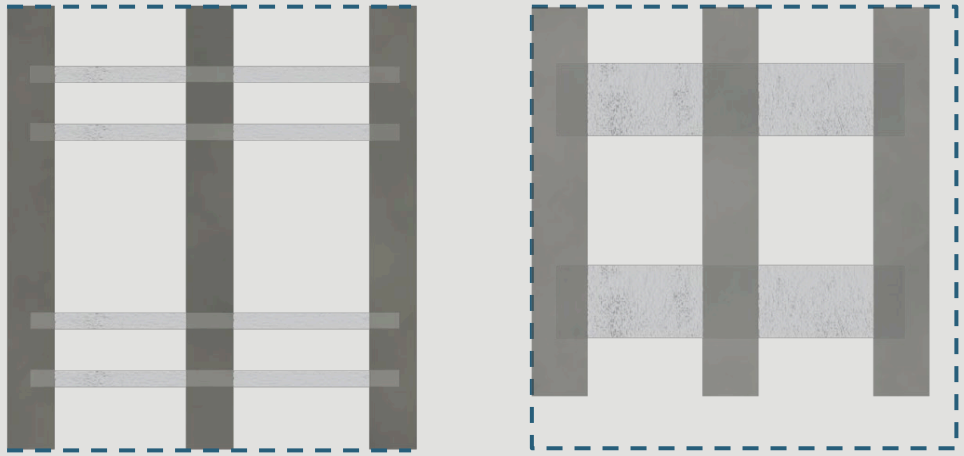
1. Depending on backside power scheme

Area and Performance Scaling with Gate-All-Around (GAA)

Reduces cell area by 20-30%

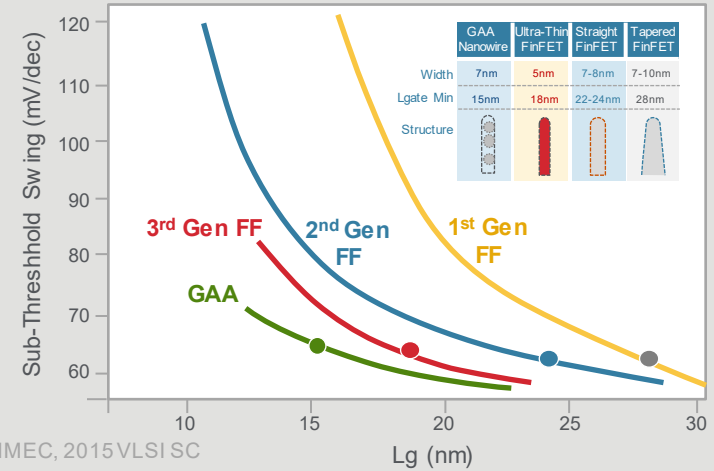


Standard cell layout and area



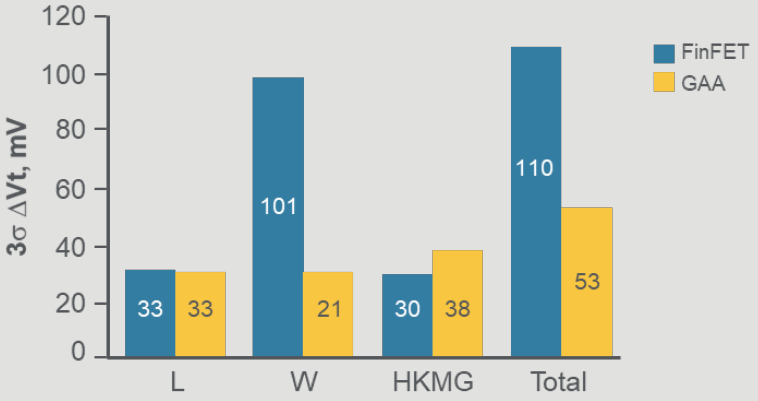
Source: Jin Cai, TSMC, 2021 VLSI SC

Reduces leakage current



Source: A. Thean, IMEC, 2015 VLSI SC

Reduces transistor variability

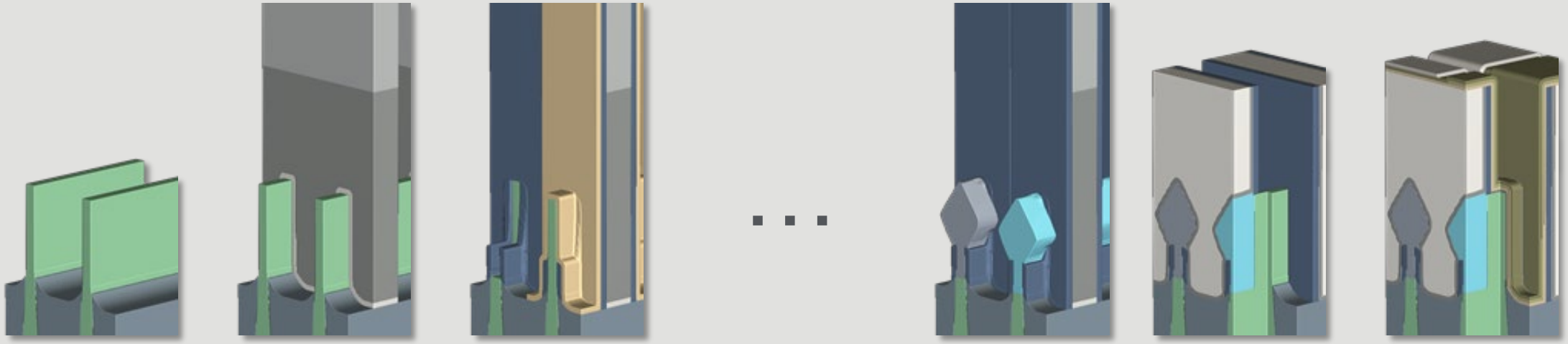


Source: SC Song, VLSI 2019

FF: FinFET
L_g: Gate Length
L: Transistor Length
W: Transistor Width
HKMG: High-K Metal Gate
ΔV_t: Threshold Voltage Shift

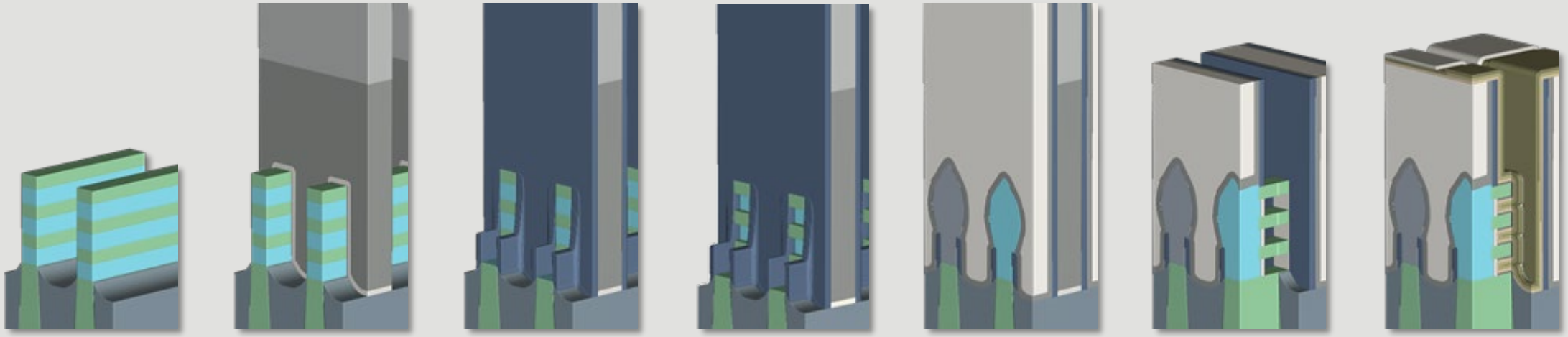
Key Steps in Gate-All-Around Fabrication

FinFET



Fin Patterning | Gate Patterning | SD Recess | . . . | pFET + nFET EPI | Poly Removal | High-k RMG

GAA

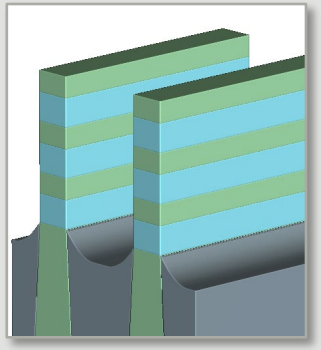


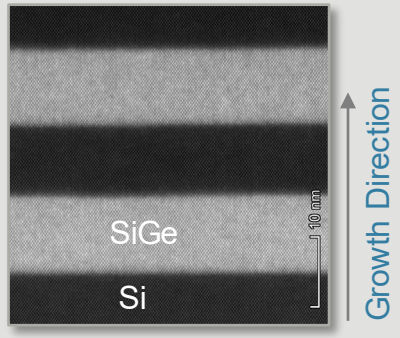
Nanosheet Patterning | Gate Patterning | SD Recess | Inner Spacer Recess | pFET + nFET EPI | Poly Removal + Channel Release | High-k RMG

pFET: p-type Transistor
nFET: n-type Transistor

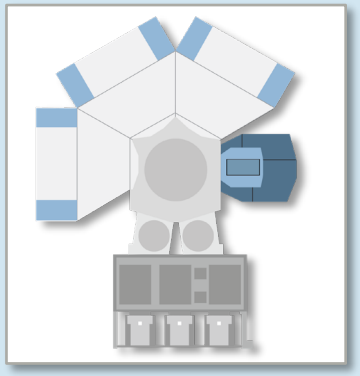
Epitaxial Steps in Gate-All-Around

Nanosheet Epitaxy - Abrupt Interfaces

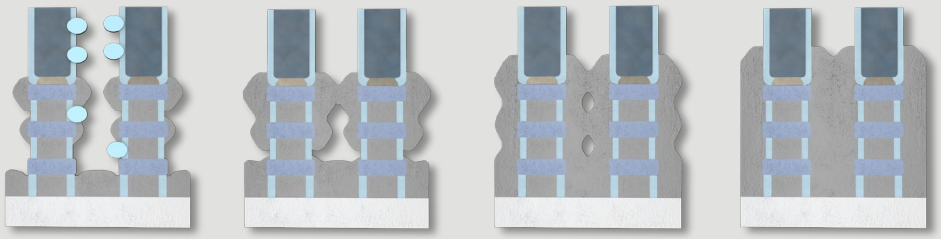




- Alternate layers of Silicon and Silicon-Germanium
- Abrupt interfaces between layers is critical
- Needs low temperature in-situ surface preparation
- Relatively fast, non-selective EPI process

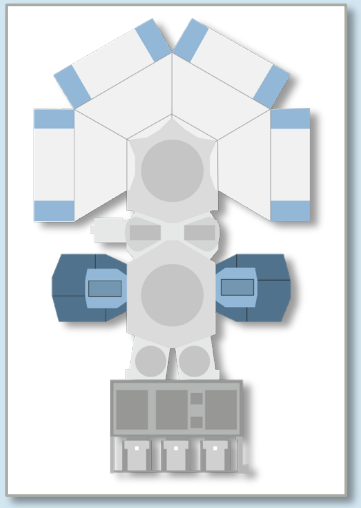


Source & Drain Epitaxy - Defect Free Growth



Epi nodules on dielectrics | Epi early merging | Void formation | Twins/ Stacking fault

- Selective epitaxy critical to device performance
- Advanced selective cleans prepare surface while protecting multiple materials
- Aspect ratio increases by 2x over FinFET dramatically increasing epitaxy complexity
- NMOS and PMOS regions processed separately



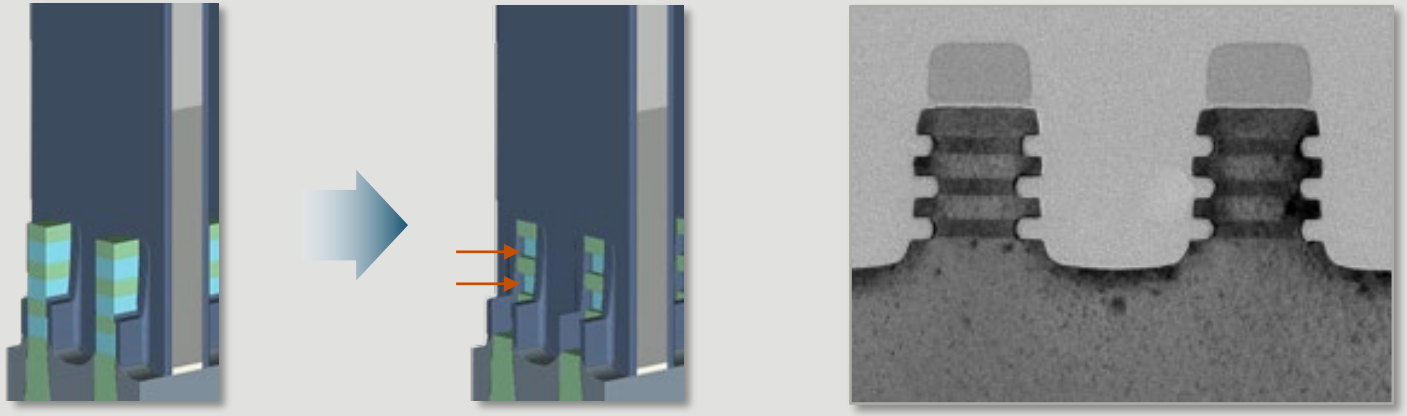
Source: Applied Materials

Applied Leadership Product: Applied Centura® Prime® Epi

NMOS: n-type transistor area
PMOS: p-type transistor area

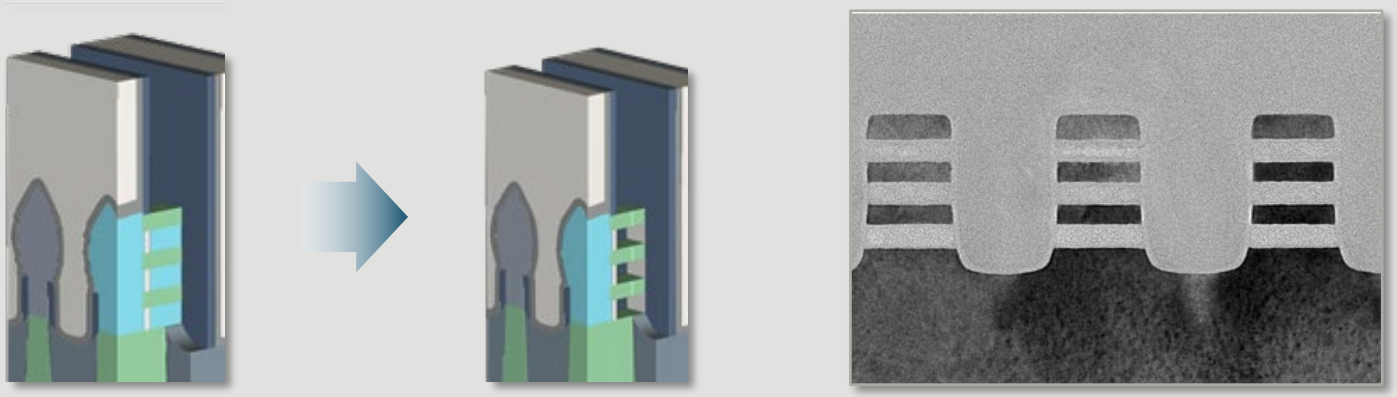
Selective Removal Steps in Gate-All-Around Fabrication

Inner Spacer Recess



- Isolates the gate from the source / drain
- Tunable SiGe to Si selectivity precisely sculpts recess profile
- No damage to surrounding materials

Channel Release



- Selective removal of SiGe defines channel width
- Extreme SiGe to Si selectivity to optimize profile

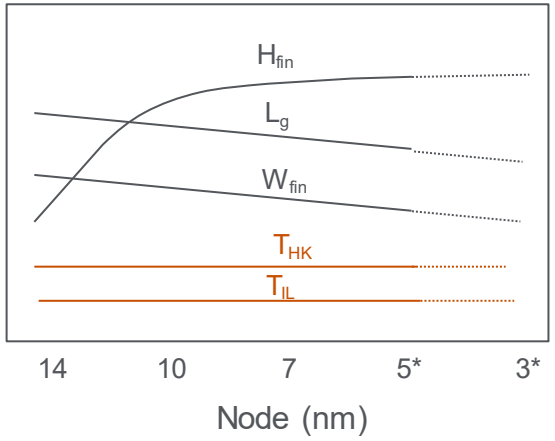
Producer® Selectra® Selective Etch
Market-leading selective etch technology

Source: Applied Materials

Resuming Gate Oxide Scaling in Gate-All-Around Transistors

EOT scaling stalled

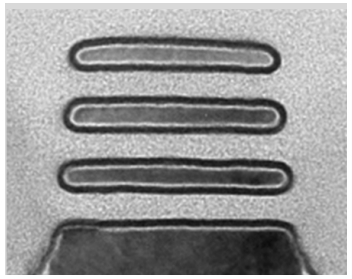
Critical transistor gate dimensions



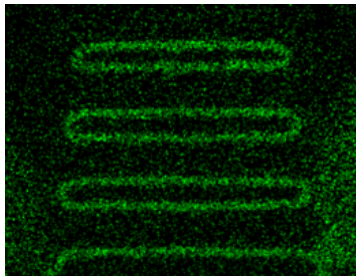
Source: S. Mahapatra, IRPS 2013

EOT scaling thru interface engineering

Conformal ALD and treatments



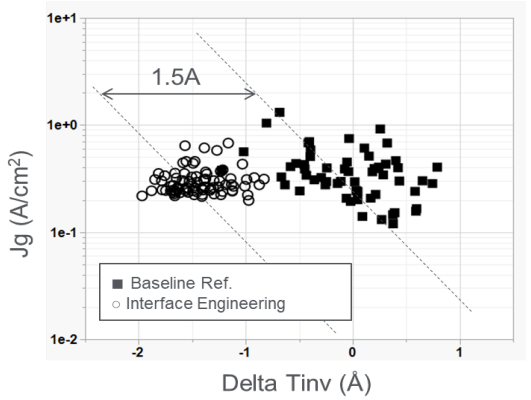
TEM contrast



Nitrogen distribution

Source: S. Hung, VLSI 2021

Thinner gate oxide at equivalent leakage



Source: S. Hung, VLSI 2021

- Gate oxide scaling boosts transistor drive current and suppresses leakage
- Further physical scaling was limited by transistor reliability

- Applied's IMS Gate Oxide solution engineers a dense interface layer with ALD high-k deposition and thermal and plasma treatment steps
- Vacuum integration, including metrology, ensures interface control
- Performance has been validated on both FinFET and GAA transistors

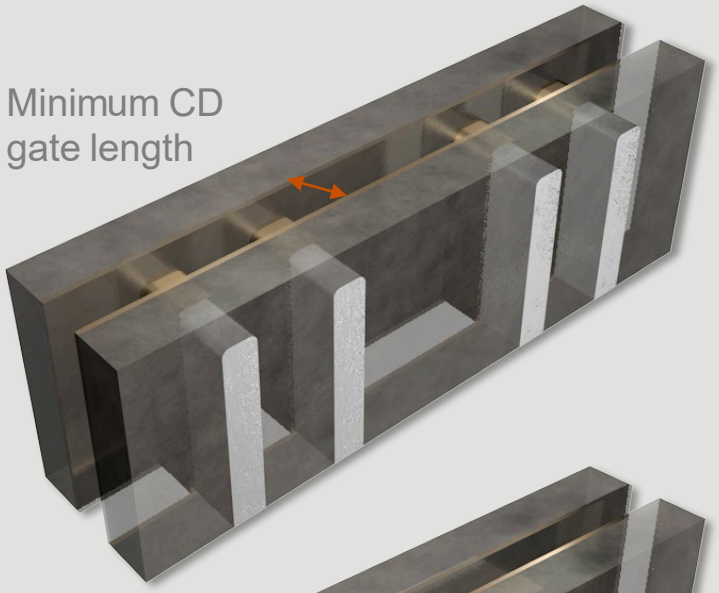
EOT: Equivalent Oxide Thickness
ALD: Atomic Layer Deposition
TEM: Transmission Electron Microscopy

J_g: Gate Leakage Current Density
T_{inv}: Inversion Layer Thickness

Engineering All-Around Metal Gates in Narrow Geometries

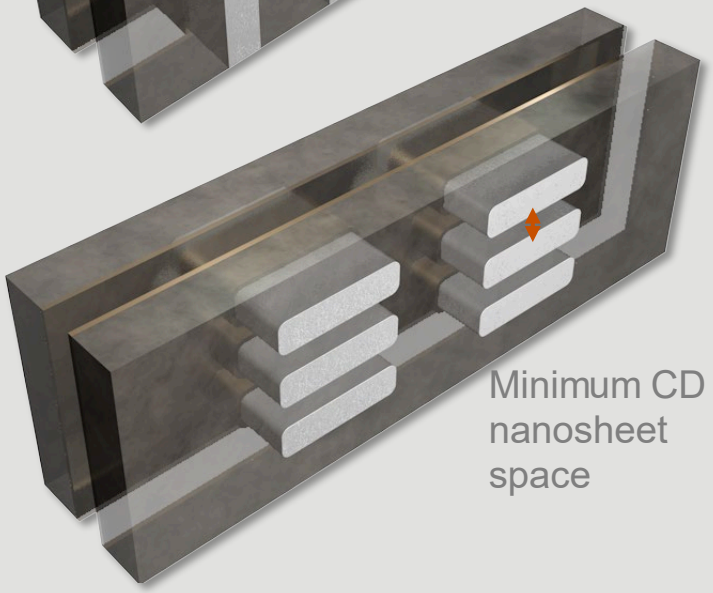
FinFET

Vt control through work function thickness tuning



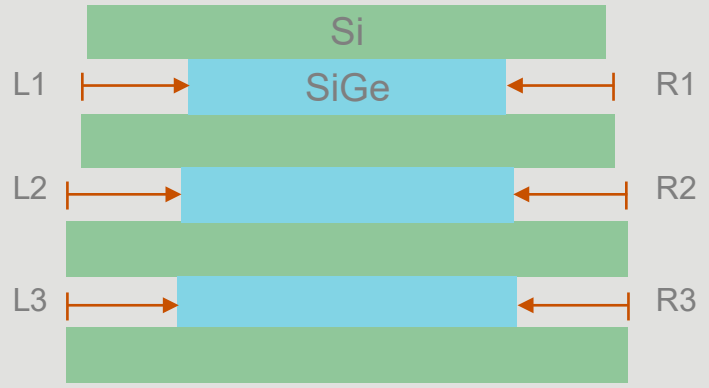
GAA

Vt control through volume-less dipole tuning



Inspection and Process Control in 3D for Gate-All-Around

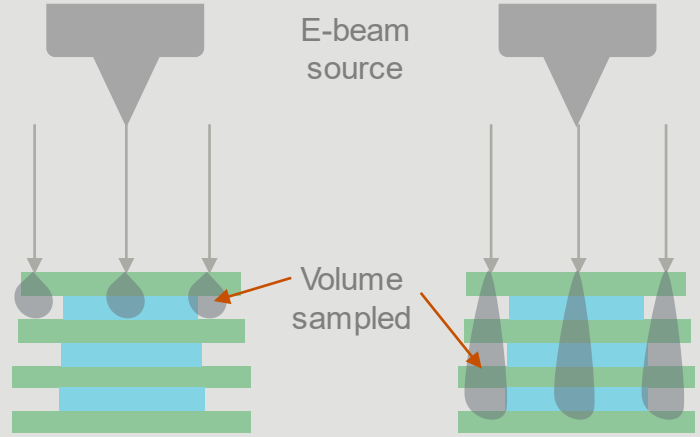
GAA process control challenges



Recess = Average of TEM (L1, L2, L3, R1, R2, R3)

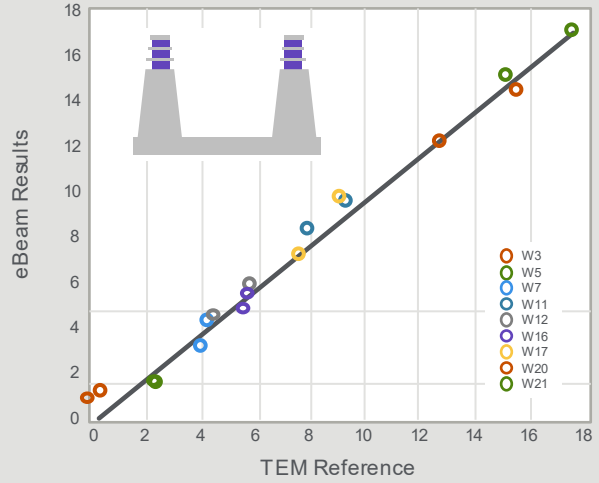
- Critical 3D features difficult to inspect and measure
- Conventional TEM analysis is expensive, destructive and slow

Measurements in 3D with electron beam see-through metrology



Low energy samples top surface

High energy samples deeper features



eBeam measurements are highly correlated to TEMs

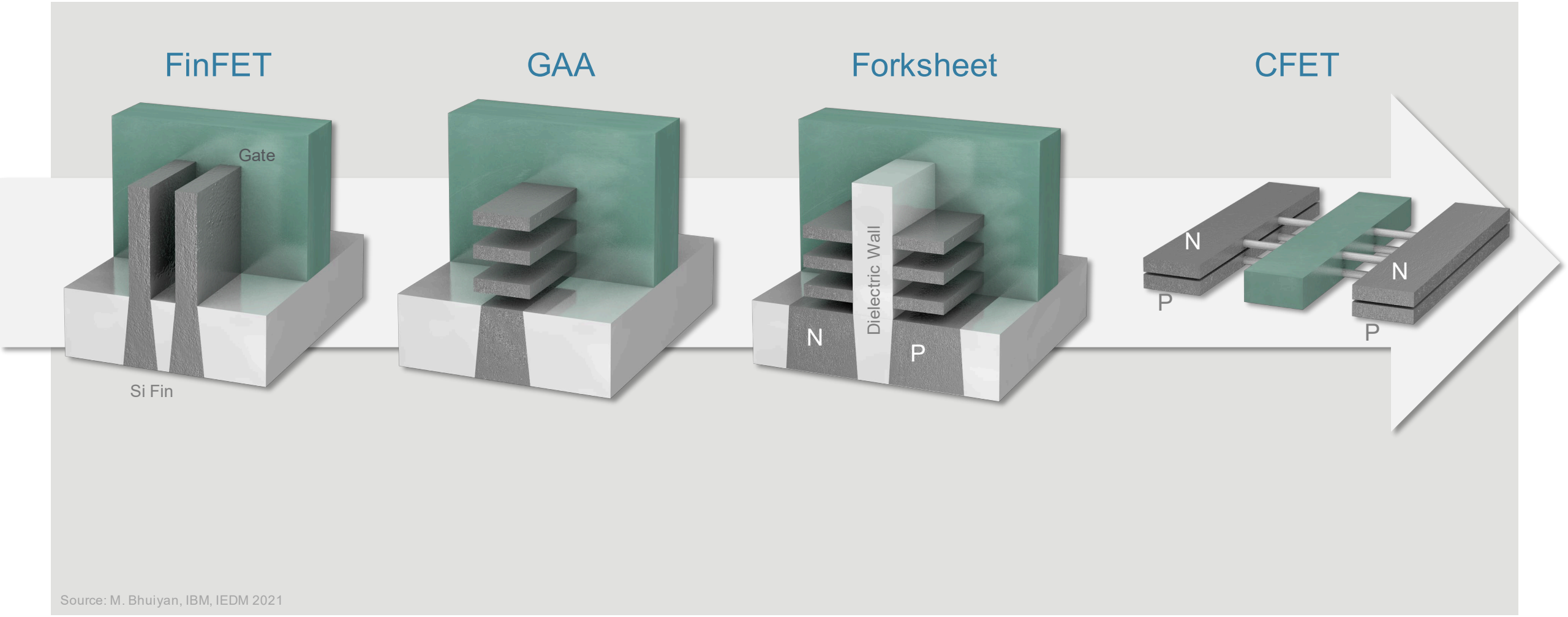
- High fidelity images across many layers
- Enables massive sampling and fast turnaround vs. TEM
- Accelerates measurements and process optimization

Applied Leadership Product: Applied PROVision® 3E eBeam Metrology System with Elluminator® Technology

Source: O. Adan, K. Houchens, Proc. SPIE, 10959, 2019

eBeam: Electron Beam
TEM: Transmission Electron Microscopy

Transistor Architecture Evolution after FinFET



Source: M. Bhuiyan, IBM, IEDM 2021

Transistor roadmap promises both area scaling and performance gains

CFET: Complementary Field Effect Transistor

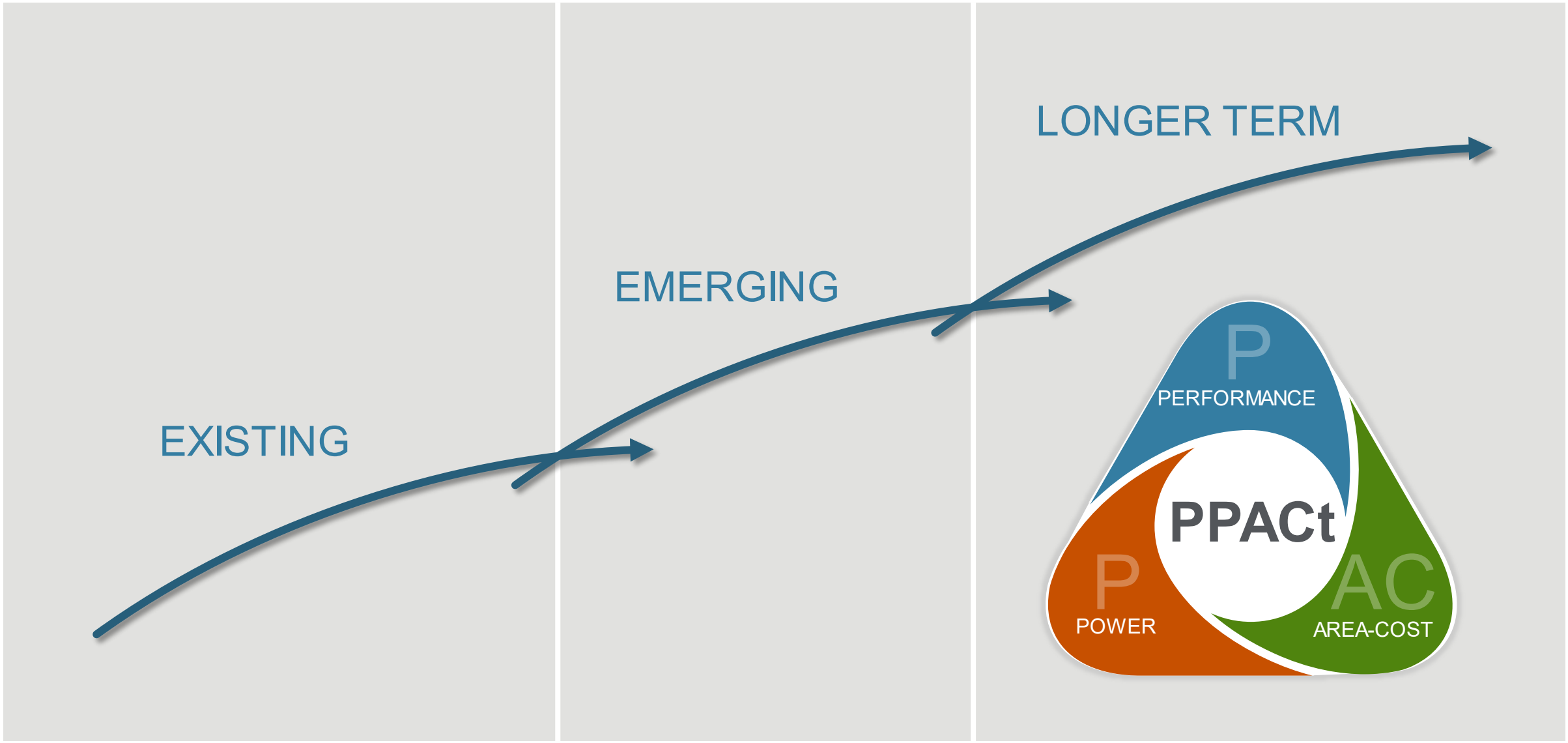
APPLIED MATERIALS®
make possible

Growth Opportunities In EUV Enablement, DTCO and Gate-All-Around

Raman Achutharaman, Ph.D.
Group Vice President
Semiconductor Products Group

NEW WAYS TO SHRINK MASTER CLASS | April 21, 2022

Inflections Over Time

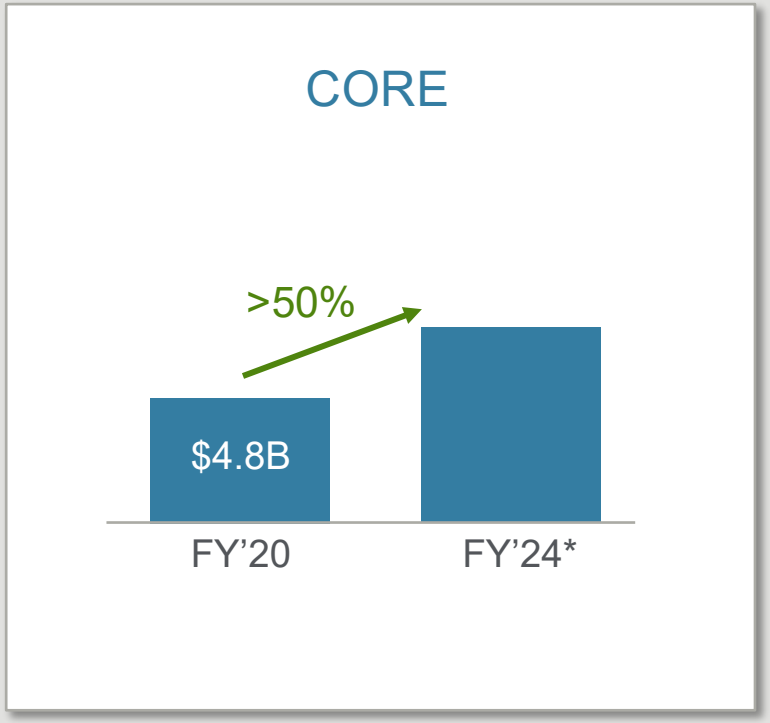


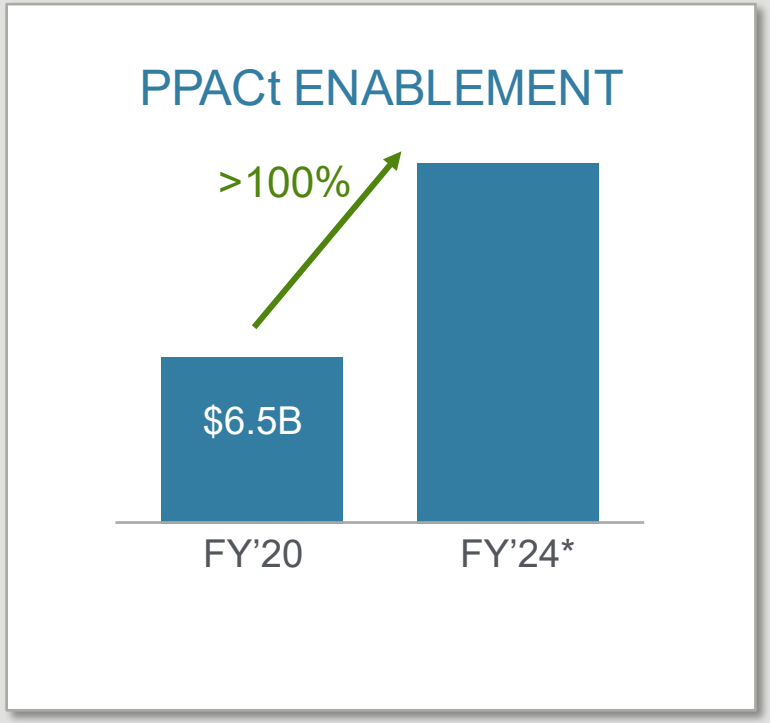
2024 Financial Model

		FY'20	FY'24 MODEL		
			LOW	BASE	HIGH
	Revenue	**$17.2B**	**$23.4B**	**$26.7B**	**$31.0B**
	Semi Systems	$11.4B	$16.2B	$18.4B	$21.7B
	Services	$4.2B	$5.6B	$6.1B	$6.7B
	Display	$1.6B	$1.6B	$2.2B	$2.7B
NON-GAAP ADJUSTED*	**GM%**	**45.1%**	**47.5%**	**48.5%**	**48.8%**
NON-GAAP ADJUSTED*	**OP%**	**26.3%**	**30.6%**	**32.4%**	**32.7%**
NON-GAAP ADJUSTED*	**EPS**	**$4.17**	**$7.00**	**$8.50**	**$10.00**

2024 model assumes non-GAAP adjusted tax rate of 12.0% and weighted average shares of 875M.
*Assumes non-GAAP adjustments as applicable for future periods. For reconciliation of GAAP to non-GAAP measures, see appendix of this presentation.

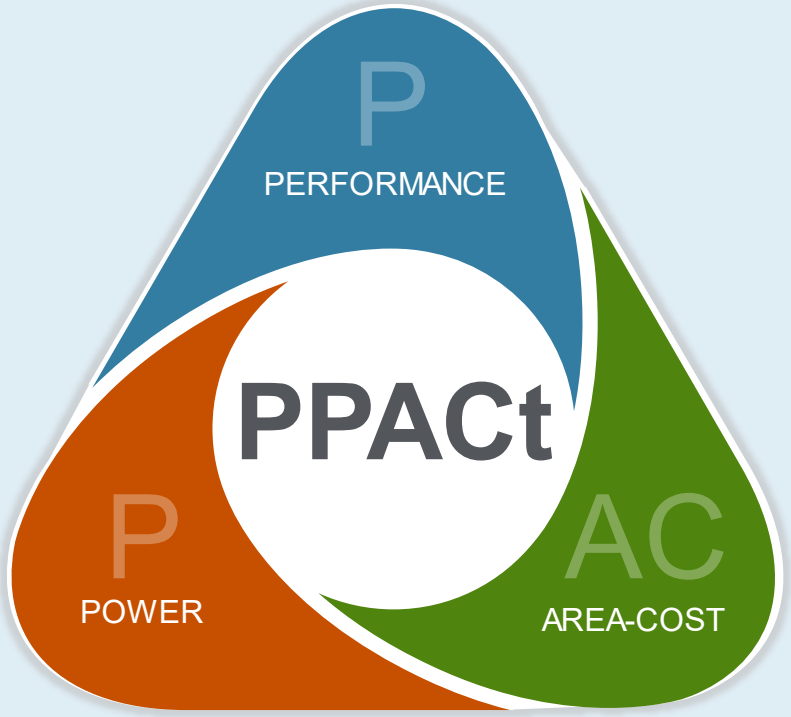
Semi Systems Revenue Growth Drivers





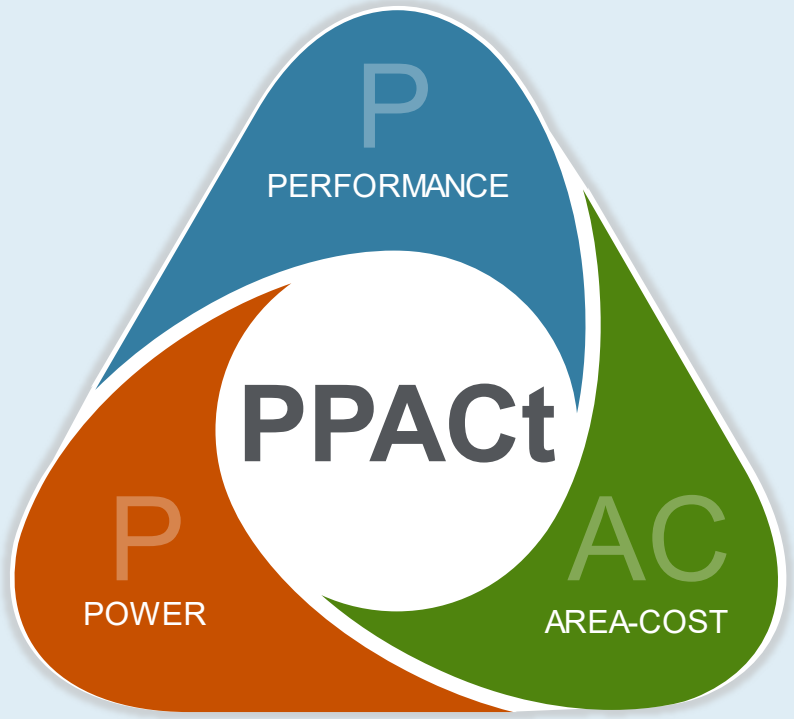
*Represents 2024 Financial Model High Scenario

The New Playbook



Enabled by	Key Inflections
New architectures	▪ New ASICs and accelerators ▪ New memory / in-memory compute ▪ Specialty, CIS, power
New structures / 3D	▪ GAA transistors ▪ Backside power distribution ▪ 3D NAND, 3D DRAM
New materials	▪ Gate ▪ Contact ▪ Interconnect
New ways to shrink	▪ EUV enablement ▪ Materials-enabled patterning
Advanced packaging	▪ High-bandwidth memory ▪ 2.5D silicon interposer ▪ 3D TSV, hybrid bonding
Time to market	▪ Process control ▪ AI^{x}™

The New Playbook



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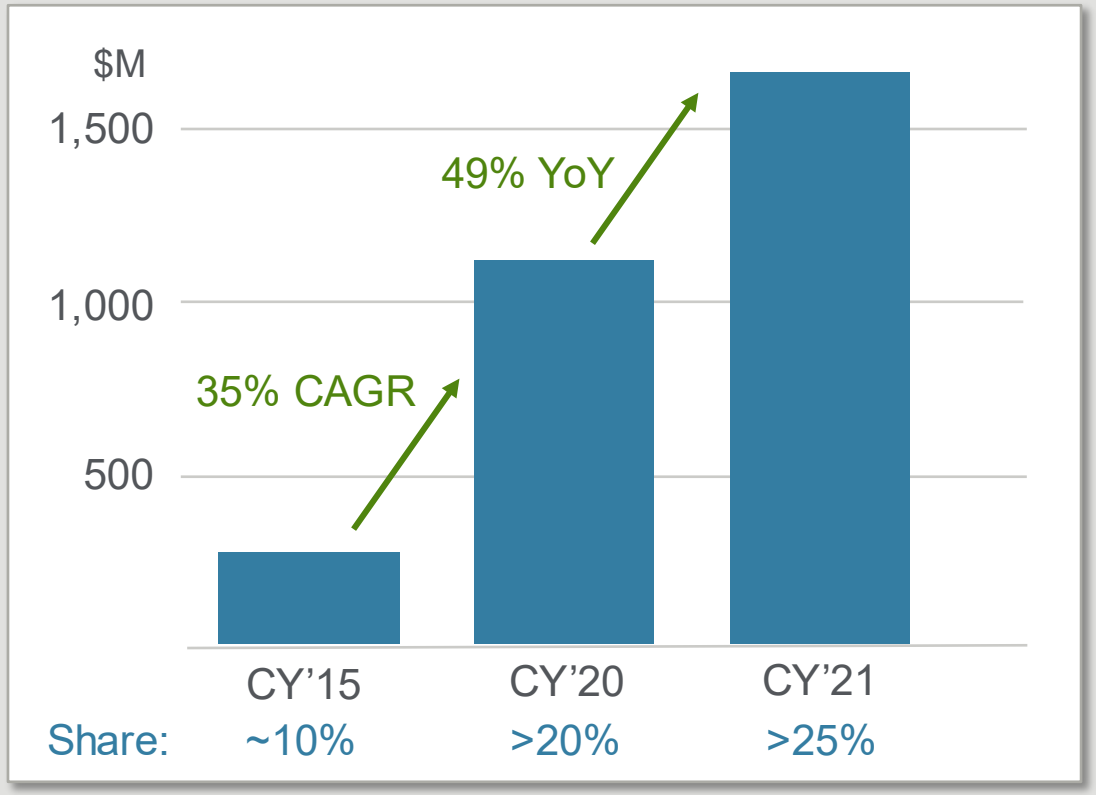
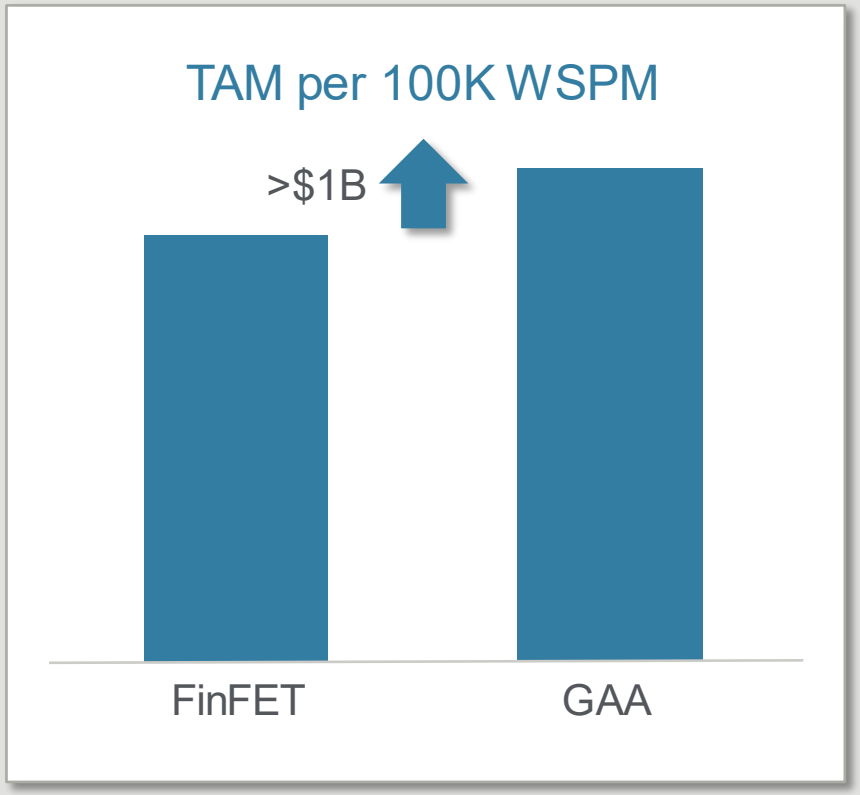
Patterning Revenue Growth



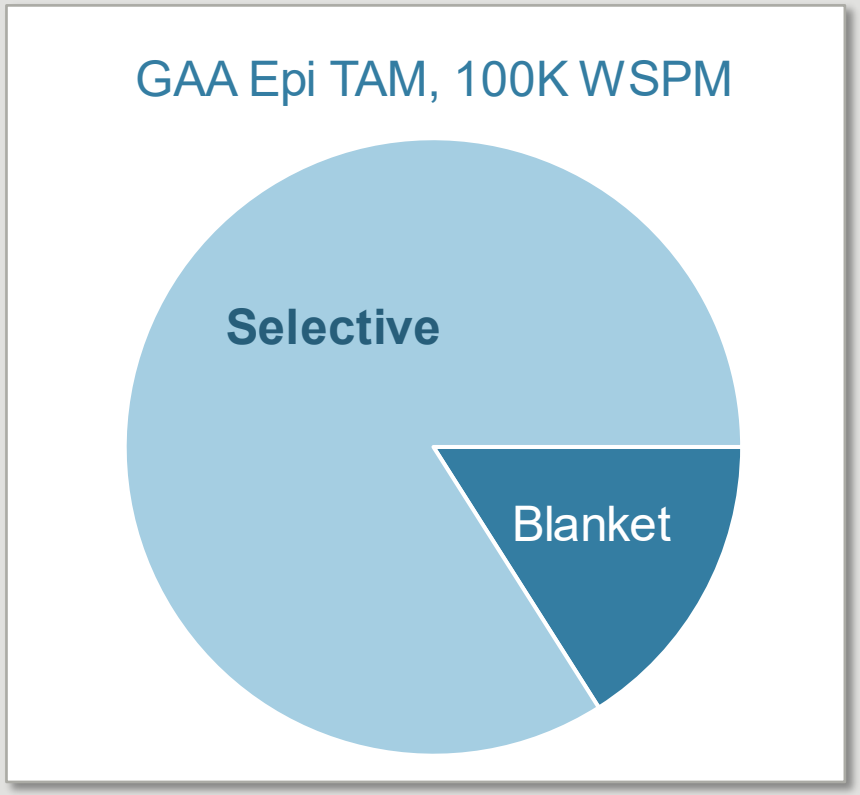
- Applied's DRAM and logic patterning markets
  - » Etch, selective removal, CVD, ALD, CMP, thermal processing
- Gaining patterning etch share in the EUV inflection
  - » +12 pts CY'15 → CY'21
- Applied is #1 in DRAM conductor etch

Gate-All-Around Increases Revenue Opportunity



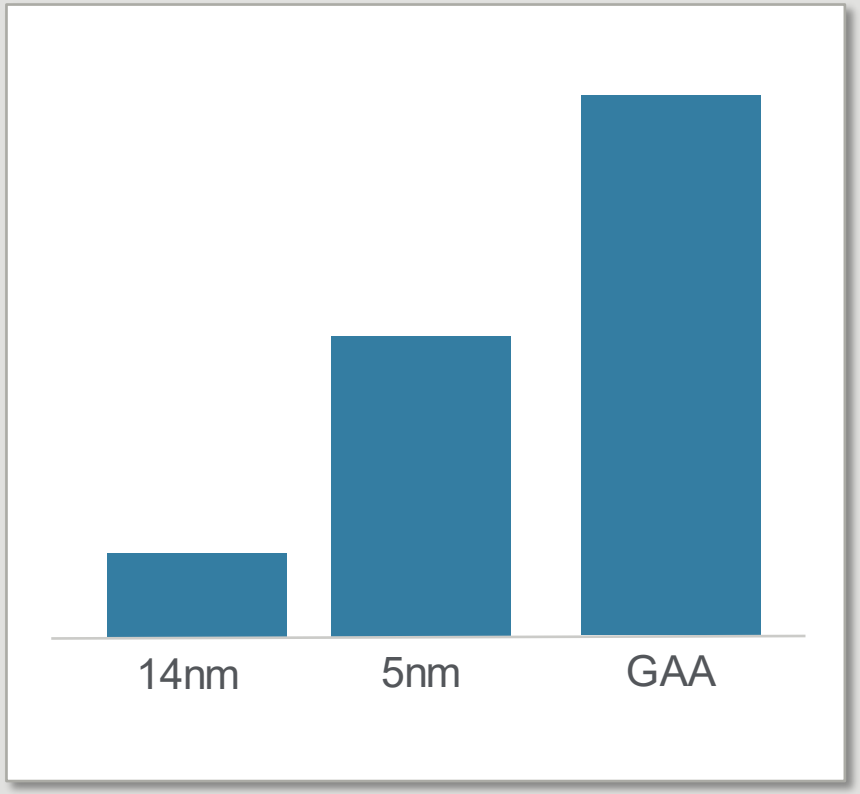
- GAA increases Applied's TAM by >$1B per 100K WSPM capacity
- Broadest GAA portfolio
  - » Epi
  - » ALD
  - » CVD
  - » PVD
  - » Etch
  - » Selective removal
  - » CMP
  - » Implant
  - » Thermal processing
  - » Process control

Gate-All-Around – Epitaxy Opportunity



- Two new expitaxy applications
  - » Rapid, blanket epitaxial deposition for GAA channel superlattice formation
  - » Precise, selective epitaxial growth for GAA channel source-drain engineering

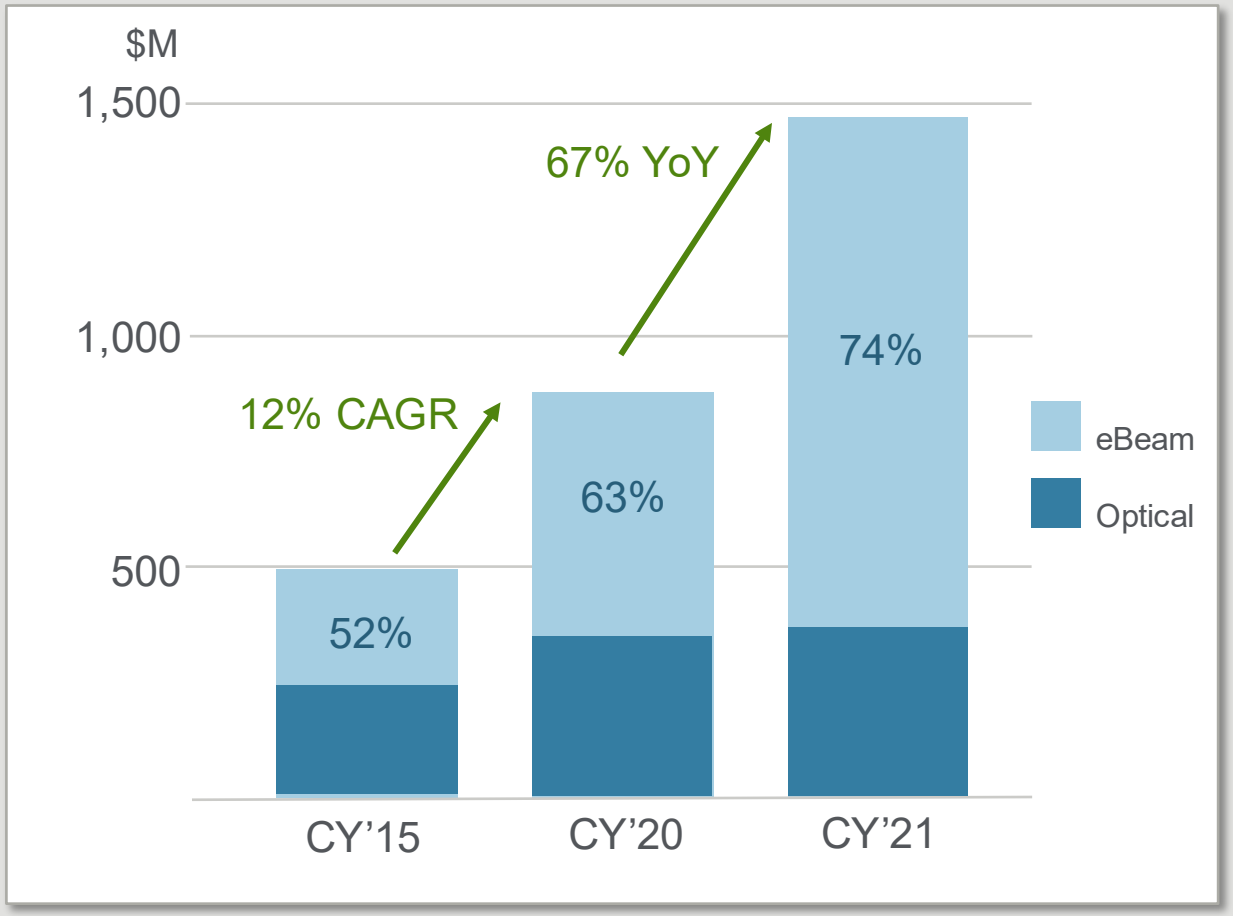
Gate-All-Around – Selective Materials Removal Opportunity



*Total SMR Steps, Leading Foundry/Logic Customers

- Selective removal helps engineer channel width and uniformity
  - » Key to chip power and performance
- Applied is capturing the majority of GAA selective etch positions
- Industry leader with >1,000 Selectra™ chambers in the field

Applied's Growth in Process Control



- Applied PDC revenue growth is accelerating and outpacing the market
- eBeam inflection expands Applied's TAM
- Applied's eBeam revenue nearly doubled in 2021
  - » VeritySEM for CD uniformity
  - » PROVision for 2D and 3D metrology and inspection
  - » SEMVision for defect review

Going Beyond Unit Process Tools to Deliver Solutions

FASTER TIME TO MARKET, HIGHER VALUE, STICKIER

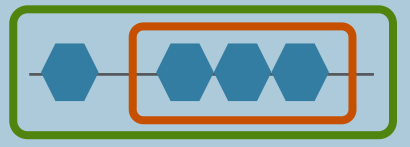
UNIT PROCESS LEADERSHIP + BROADEST PORTFOLIO

CO-OPTIMIZATION OF PROCESSES / TOOLS

~40% of our products now co-optimized

INTEGRATED MATERIALS SOLUTIONS

~30% of our products now integrated



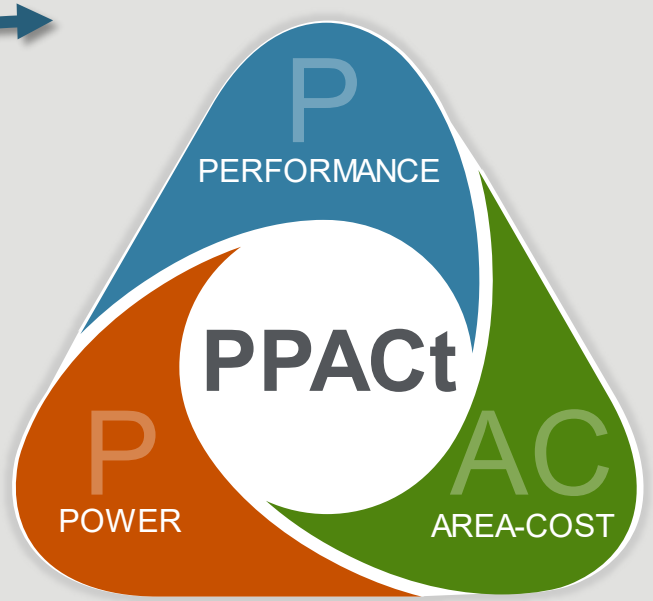
ACTIONABLE INSIGHT ACCELERATION

Inflections Over Time

EXISTING
- EUV Enablement
- eBeam Metrology
- Wiring
- DRAM HKMG

EMERGING
- Gate-All-Around
- Backside Power
- Hybrid Bonding

LONGER TERM
- 3D DRAM
- Forksheet
- CFET



* Partial list of key inflections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