PANEL DISCUSSION DURING IEDM 2023

December 12, 2023 at 5:00 PM PT
Hotel Nikko, San Francisco

NICK YU

Custom Silicon Technologist
Google

Nick Yu is an engineering leader in SoC product development. Nick joined Google 5 years ago as Custom Silicon Technologist. Nick has over 30 years of experience riding Moore's Law in SOC product designs and collaborating with the semiconductor supply chain to tackle all the design complexities that got in the way.

Nick has worked at Qualcomm previously, spending 10+ years in SoC architecture & design; 10 years in semiconductor supply chain engineering development; and 5 years at Quacomm Research working on advanced semiconductor & systems architecture such as novel memory technologies, 3D integration and ultra low power technologies.

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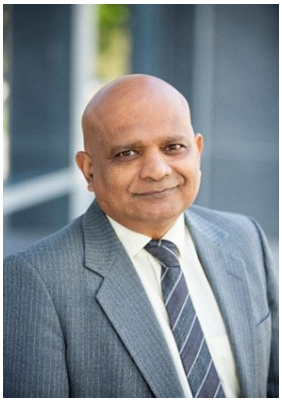

PR “CHIDI” CHIDAMBARAM

Vice President
Engineering
Qualcomm

PR. Chidi Chidambaram leads the process technology engineering team at Qualcomm as Vice President of Engineering and is recognized as Qualcomm Fellow.

Qualcomm is a leader in the fabless industry – introducing leading-edge semiconductor technologies to manufacturing. Qualcomm was the first company to ship large volume products in 10nm technology in 2017. In addition to the leading-edge CMOS technologies, Chidi’s team is also responsible for RF devices based on FinFET and SOI transistors.

Before joining Qualcomm, Chidi developed silicon technology at Texas Instruments and was instrumental in the first embedded SiGe implementation by the semiconductor industry. He is also recognized by IEEE as a fellow for his contribution to strain engineering and design technology co-optimization (DTCO). In his 20+ year semiconductor career, evenly distributed between research and development, Chidi has written and earned over 100 referred articles and patents each.

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KEVIN FISCHER

Vice President
Intel Corporation

Kevin Fischer is Vice President and Director of Interconnect and Memory Technology Integration in Logic Technology Development at Intel. His current role is managing technology development as program manager for the Intel 20A and Intel 18A technologies. His team is responsible for all aspects of technology development of Intel's lead technology to combine RibbonFET transistors along with PowerVias and backside power.

Prior to this role, he worked as program manager on Intel's eNVM project developing MRAM and RRAM and prior to that he managed Intel's 14nm program development in HVM. He started his career at Intel in 2000 as an interconnect process integration engineer and later as an interconnects program lead. As an interconnect engineer his accomplishments include the introduction of technologies into Intel's logic technology including: the first HVM logic technology air gap interconnect, Intel's embedded MIM capacitor and Intel's first spacer based pitch division for interconnects. He has worked on every Intel technology since 90nm in some capacity.

Kevin received his Ph.D degree in electrical engineering from the University of Wisconsin at Madison and his electrical and computer engineering B.S./M.S. degrees there as well. Kevin holds over a dozen US patents and has published over 30 papers in accredited journals and conferences in semiconductor technology and related fields.

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DONG-WON KIM

Fellow, Logic Technology Development

Samsung

Dr. Dong-Won Kim is a Fellow of Logic Technology Development, Semiconductor R&D Center, in charge of logic device development for 3nm and beyond 3nm node. His research & development focused on the nano scaled device, 3 & 1 dimensional CMOS transistors, and 20nm, 14nm, 10nm, & 7nm technology node for logic device applications. He has authored or coauthored over 110 publications related to nano scale device, especially FinFET, GAA (Gate All Around) device, alaso known as MBCFET (Multi-Bridge Channel FET) and Logic applications. He played a pivotal role in its development and contributed significantly to product development. He is the holder of over 114 U.S. patents, including MBCFET origin patent. He had severed on several IEEE conference technical committees including IEDM, SOI conference, ICICDT, VLSI-TSA and Silicon Nanoelectronics Workshop.

He received the B.S. and M.S. degrees from Korea University, Seoul, Korea in 1987 and 1997, respectively, and the Ph.D. degree at the University of Texas, Austin in 2003.

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GEOFFREY YEAP

VP, Research & Development

TSMC

Geoffrey Yeap received the BSEE, MSEE, and Ph.D. degrees in electrical and computer engineering with a specialization in microelectronics from The University of Texas at Austin, Austin, TX, USA, in 1986, 1988, and 1994, respectively. He was a Vice President of Engineering at Qualcomm Technologies Inc., in charge of silicon technology and foundry engineering (advanced digital CMOS, RF/analog, PMIC and bump/CPI) and foundry IP/design enablement. He has more than 25 years of semiconductor industry experience working at TSMC, Qualcomm, Motorola, and Advanced Micro Devices on advanced high-performance microprocessor and mobile silicon technology development, new technology/product introduction, as well as design/technology co-optimization. He is currently working at TSMC, Hsinchu, Taiwan, on the flagship advanced technology platform. He has authored more than 55 refereed journal/conference articles and holds more than 90 U.S. and international patents.

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VICTOR MOROZ

Fellow

Synopsys

Dr. Victor Moroz is a Synopsys Fellow, engaged in a variety of projects on modeling Design-Technology Co-Optimization, FinFETs, gate-all-around transistors, stress engineering, 3D ICs, transistor scaling, cryogenic devices, Middle-Of-Line and Back-End-Of-Line resistance and capacitance, solar cell design, innovative patterning, random and systematic variability, junction leakage, non-Si transistors, and atomistic effects in layer growth and doping.

Several facets of this activity are reflected in three book chapters, 100+ technical papers and over 300 US and international patents. Victor has been involved in technical committees at ITRS, IEDM, SISPAD, DFM&Y, ECS, IRPS, EDTM, and ESSDERC, including serving as a Technical Chair of SISPAD 2018 and is currently serving as an Editor of IEEE Electron Device Letters.

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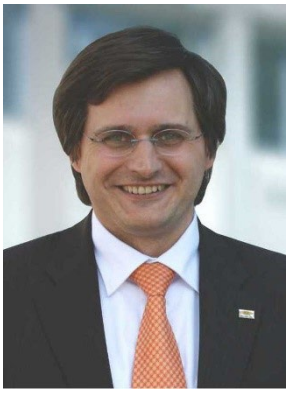

PAUL LINDNER

Executive Technology Director
EV Group

Paul Lindner is EV Group's executive technology director. He heads the R&D, product and project management, quality management, business development and process technology departments. Customer orientation throughout all steps of product development, innovation and implementation in a production environment are among the main goals of EV Group's technology groups headed by Paul.

Paul joined the company in 1988 as a mechanical design engineer and has since pioneered various semiconductor and MEMS processing systems, which have set industry standards. His responsibilities included the design of semiconductor processing systems and tooling for custom applications, including innovative system designs pioneered in the first commercially available wafer bonders, silicon-on-insulator (SOI) bonding systems and precision alignment systems for 3D interconnect applications. Prior to his appointment as executive technology director, Paul established a product management department at EV Group. During that time he was involved in marketing, sales, manufacturing and on-site process support.

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BALA HARAN

Vice President
Semiconductor Products Group
Applied Materials

Dr. Bala Haran is Vice President of Integrated Materials Solutions at Applied Materials where he leads a team of device integrators and process engineers focused on identifying and enabling new inflections in logic and memory technology.

Prior to joining Applied, Bala was at IBM for 18 years where he led multi-company process and device integration teams focused on CMOS technology development and transfer. He holds a Ph.D. in chemical engineering from the University of South Carolina and has more than 50 peer-reviewed publications and 100 patents granted.

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