APPLIED MATERIALS®

LOGIC MASTER CLASS

JUNE 16, 2021

Forward-Looking Statements and Other Information

Today's presentations contain forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our investment and growth strategies, our development of new products and technologies, our business outlook for fiscal 2021 and beyond, the impact of the ongoing COVID-19 pandemic and responses thereto on our operations and financial results, strategic acquisitions and investments, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic and industry conditions; the effects of regional or global health epidemics, including the severity and duration of the ongoing COVID-19 pandemic; global trade issues and changes in trade and export license policies, including the recent rules and interpretations promulgated by the U.S. Department of Commerce expanding export license requirements for certain products sold to certain entities in China; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; acquisitions, investments and divestitures; changes in income tax laws; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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2021 Master Classes

WELCOME

Michael Sullivan
CVP, Head of Investor Relations

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UPCOMING INVESTOR EVENTS

MASTER CLASSES

April 6	May 5	June 16	Second Half 2021
2021 Investor Meeting	Memory	Logic	▪ Specialty semiconductors ▪ Heterogeneous design and advanced packaging ▪ Inspection and process control

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UPCOMING INVESTOR EVENTS

MASTER CLASSES

April 6	May 5	June 16	September 8*	October 18*
2021 Investor Meeting	Memory	Logic	ICAPS & Advanced Packaging	Process Control & AIx™ Platform

* Projected Dates

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AGENDA

9:00	**PART 1**	HOST: Mike Sullivan Logic Thesis Fireside Chat | PR Chidi Chidambaram, Ph.D., Qualcomm
9:15	**PART 2**	HOST: Uday Mitra, Ph.D. Logic Technology Transistor | Michael Chudzik, Ph.D. Interconnect | Mehul Naik, Ph.D. Patterning & DTCO | Regina Freed
9:55	**PART 3**	HOST: Raman Achutharaman, Ph.D. Logic Growth Opportunities
10:05	**Q&A**	Raman, Uday, Mike

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TAKEAWAY
Messages

1. "AI Era" = **Secular growth** in logic capacity
2. **PPACt™ enablement** via the New Playbook will capture a growing proportion of WFE market growth
3. **DTCO** is a powerful way to use materials engineering to drive continued 2D scaling at existing line widths

* Free cash flow = operating cash flow – net capital expenditures
** Non-GAAP adjusted EPS

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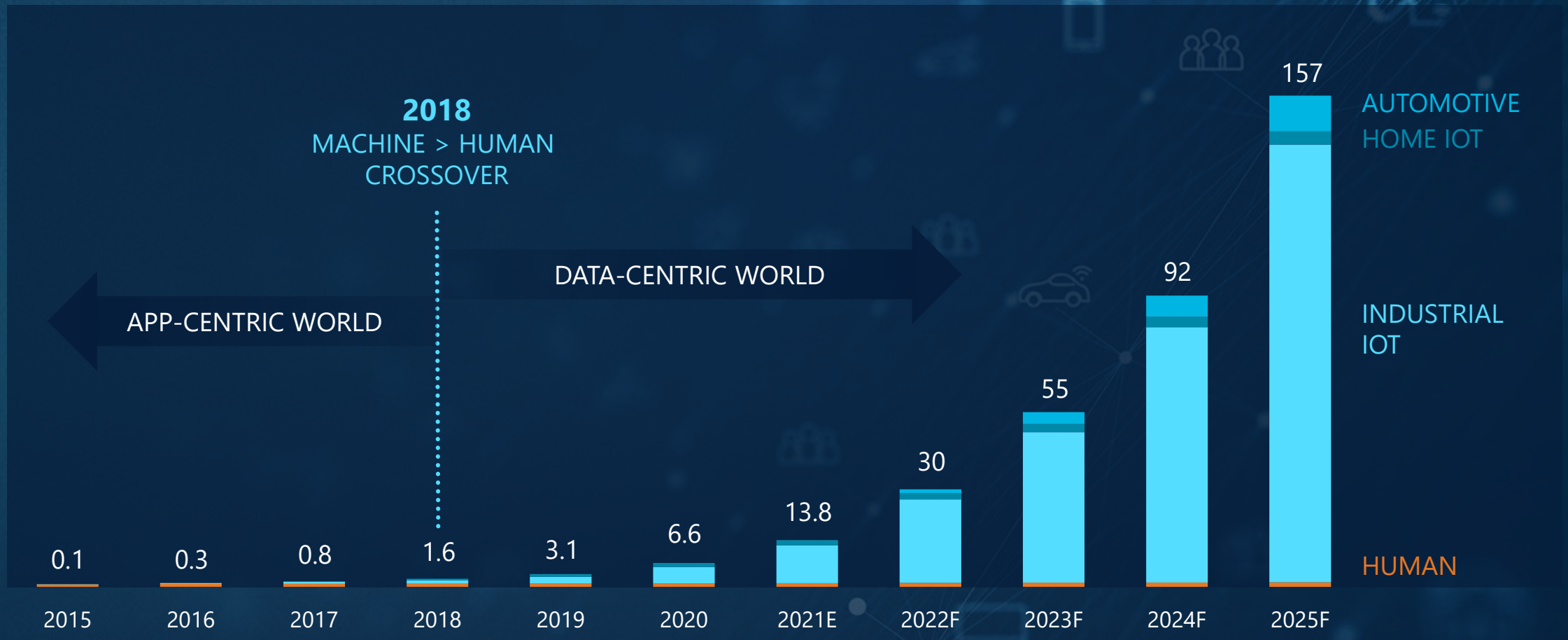
Data Generation By Category (ZB)



SEMI GROWTH NO LONGER LIMITED BY HUMAN CONSUMPTION

Source: Applied Materials

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Semi content per unit	2015	2020	2025F	
HIGH END SMARTPHONE	$100	$170	$275	+62%
AUTO (GLOBAL AVERAGE)	$310	$460	$690	+50%
DATACENTER SERVER (CPU + ACCELERATOR)	$1,620	$2,810	$5,600	+99%
SMARTHOME (GLOBAL AVERAGE)	$2	$4	$9	

SILICON CONTENT GROWING AS EVERYTHING GETS SMARTER

Source: Applied Materials

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Strong Multiyear Capital Investments

"TSMC to Spend $100 Billion Over Three Years to Grow Capacity" – Bloomberg, 3/31/2021

"Intel CEO Presses Turnaround Effort With $20 Billion Investment Plan" – The Wall Street Journal, 3/23/2021

"Samsung to Invest $115 Billion in Foundry & Chip Businesses by 2030" – AnandTech, 4/24/2019

"Samsung raises spending in logic chip businesses to $151 billion" – ZDNet, 5/13/2021

"S. Korea Gives Final Nod to SK Hynix's 120 Tln-Won Project" – Yonhap News, 3/29/2021

Incentives for Domestic Production

"Biden doubles down on a $50 billion plan to invest in chips" – Fortune, 4/13/2021

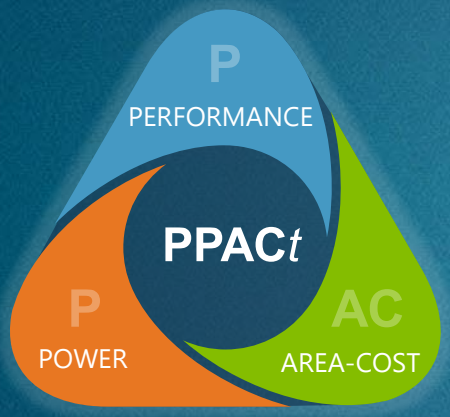
"EU aims to be independent chip power with 20% global share" – Nikkei Asia, 3/10/2021

"South Korea joins global chipmaking race with $450 billion spending plan" – Fortune, 5/13/2021

"Japan Lays Out 'National Project' for Chips After Lost Decades" – Bloomberg, 6/3/2021

"China wants to boost disruptive semiconductor technologies" – Shanghai Daily, 5/15/2021

Playbook and Growth Drivers



New architectures/ New devices	Specialty devices, mature nodes (IoT), custom ASIC
New structures/3D	Future 3D devices favoring our served markets
New materials	Low resistance metals, high-speed DRAM periphery
New ways to shrink	Materials-enabled patterning, EUV enablement
Advanced packaging	Fine-pitch interconnect for multi-chip system integration
Accelerate time-to-market	Actionable insight: eBeam, sensors + metrology + AI/ML

’20 to ’24

Rev oppty. **+$7B**

Rev CAGR 13%

WFE CAGR 8 to 9%

IoT = Internet of Things ASIC = Application-specific Integrated Circuit eBeam = Electron Beam

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Industry Papers Discuss PPACt™ and DTCO

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CONFERENCE PROCEEDINGS

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Open Access | Presentation

Select Language

Translator Disclaimer

22 February 2021

A new era for AI HPC and IC technologies in the transition to an intelligent digital world

John Hu

Abstract: "This IC technology scaling is driven by key factors such as **performance, power,** perfection (yield/reliability), **area, cost, and time to market (PPACt)**"

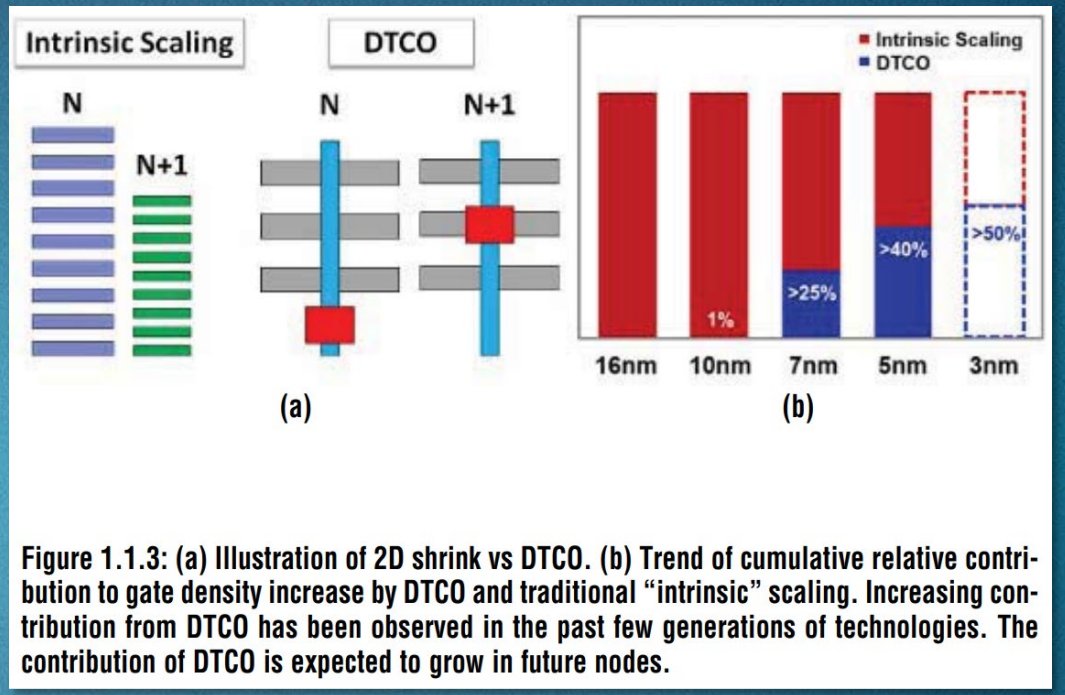

Figure 1.1.3: (a) Illustration of 2D shrink vs DTCO. (b) Trend of cumulative relative contribution to gate density increase by DTCO and traditional "intrinsic" scaling. Increasing contribution from DTCO has been observed in the past few generations of technologies. The contribution of DTCO is expected to grow in future nodes.

ISSCC, February 15, 2021
"Unleashing the Future of Innovation"
Dr. Mark Liu, Chairman, TSMC
Abstract: "**The contribution of DTCO is expected to grow in future nodes.**"

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PART 2

Logic Technology

Uday Mitra, Ph.D.
Vice President
Semiconductor Products Group

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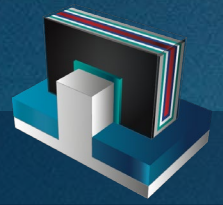
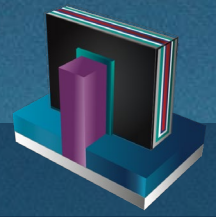
Enabling PPACt™ Roadmap for Logic

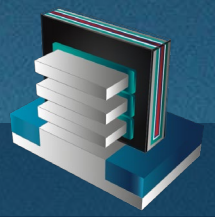


FinFET

Scaled FinFET



GAA



FOUNDRY NODE	14/16nm	10/7nm	5nm	3nm	2nm	< 2nm
	2015	2017	2019	2021	2023	2025+
CHANNEL	STI Optimization		Epi SiGe Channel	Epi Si / SiGe SL		
SD			Epi SiAs+SiP	Inner Spacer		
GATE	Conformal HKMG				Band-Edge	New Dipole
CONTACT		Co fill	Sel W MOL	Liner-free		
BEOL	Sel Co Cap	ALD Barrier		Sel ALD Barrier		Buried or Backside Power Rail
DTCO	SDB	SA-SDB	COAG			
PITCH SCALING	SADP	SAQP	EUV	EUV SADP		

GAA: Gate-All-Around
STI: Shallow Trench Isolation
HKMG: High-k Metal Gate

Sel: Selective
MOL: Middle-of-Line
ALD: Atomic Layer Deposition

SDB: Single Diffusion Break
SA-SDB: Self-Aligned Single Diffusion Break
COAG: Contact Over Active Gate

SADP: Self-Aligned Double Patterning
SAQP: Self-Aligned Quadruple Patterning
EUV: Extreme Ultraviolet Lithography

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PART 2
LOGIC TECHNOLOGY

TRANSISTOR

Michael Chudzik, Ph.D.
Vice President of Technology

INTERCONNECT

Mehul Naik, Ph.D.
Managing Director and Principal Member of our Technical Staff

PATTERNING & DTCO

Regina Freed
Managing Director of Patterning Technology

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PART 2

Logic Transistor Challenges and Roadmaps

Michael Chudzik, Ph.D.
Vice President
Semiconductor Products Group

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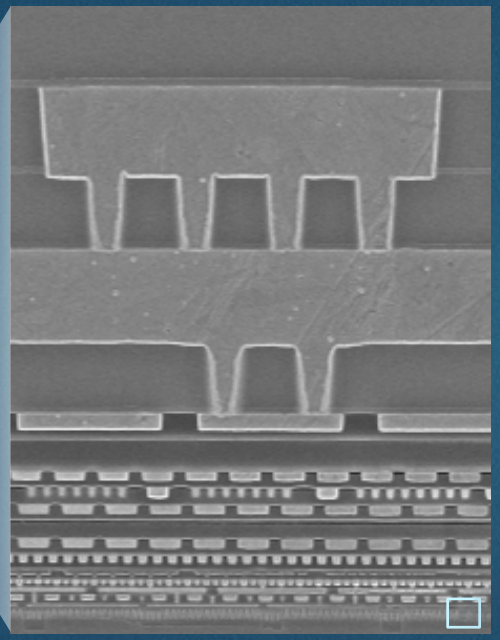
Zooming in on Smartphone Chip Transistors

Source: Apple

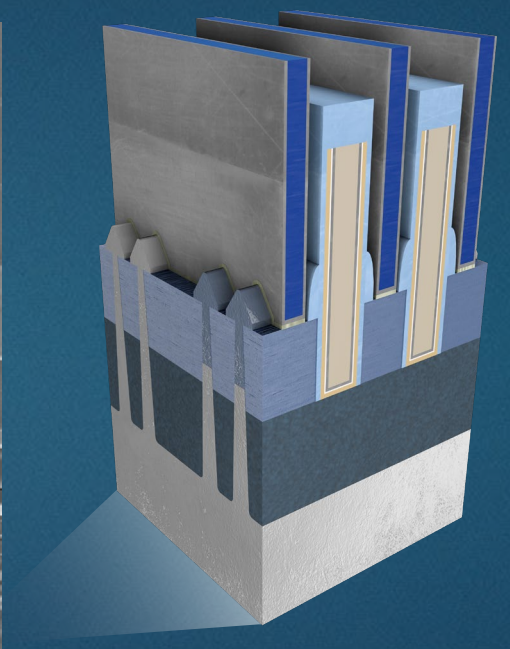
Source: Apple

Processor chip: 88mm^2 size
8.57 mm x 10.23 mm



Source: TechInsights

Microscope cross section view of chip



3D model of a transistor and contacts

5nm
technology node

>11.8 billion
transistors

>24 billion
contacts

7 threshold voltages
HPC and mobile compute

• V_T *Threshold voltage*

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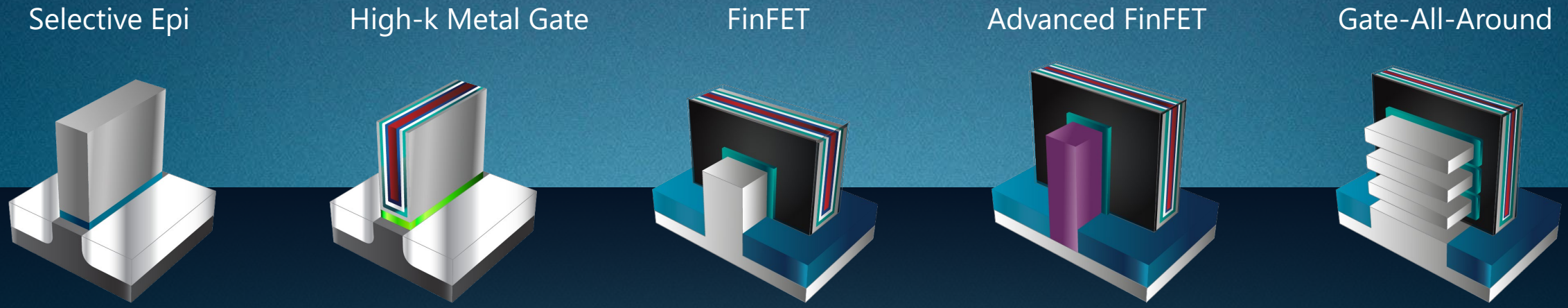
Decades of Leadership in Transistor Enablement



Unit Process Leadership

Epi
Implant
Metal Gate
RTP Anneal
CMP
Selective Removal

+

Integrated Materials Solutions Leadership

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Physics of Transistor Performance

Transistor performance

$$\text{Transistor speed} = \frac{1}{t}$$

$$\text{Delay } t = \frac{CV}{I_d} = CR$$

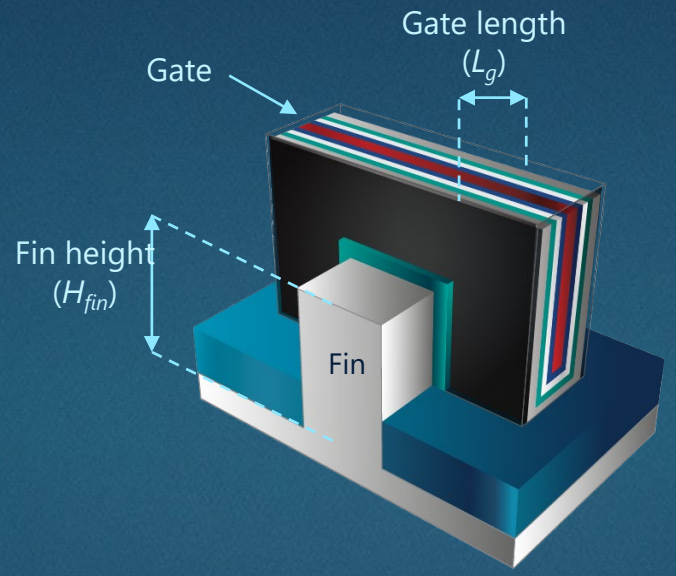
$$I_d \approx \left(\frac{H_{fin}}{L_g}\right)\frac{\mu}{t_{ox}}(V_G - V_T)^2$$

Higher drive current I_d or lower transistor resistance R & C = higher transistor speed

t Delay
C Capacitance
V Voltage
I_d Drive current
R Resistance

μ Mobility
t_{ox} Gate oxide thickness
V_G Gate voltage
V_T Threshold voltage

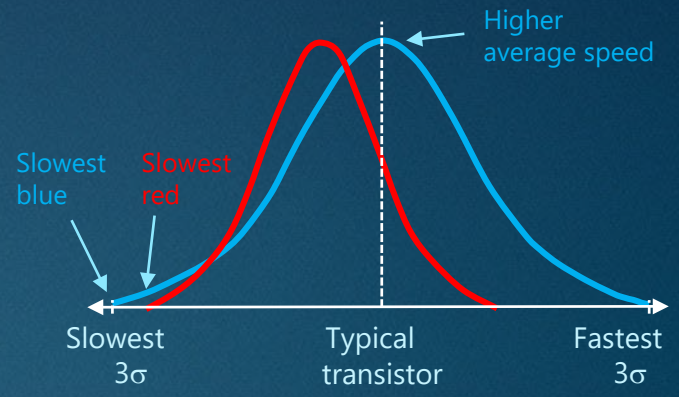
Scaling implication



I_d ↑
- Taller fins H_{fin}
- Smaller gate length L_g
- Higher mobility μ
- Thinner gate oxide t_{ox}
- Lower threshold voltage V_T

R ↓
- Activated dopant concentration

Variability implication



Greg Yeric, IEDM 2015

Speed is set by the slowest transistor

Lower transistor variability
= Higher device performance

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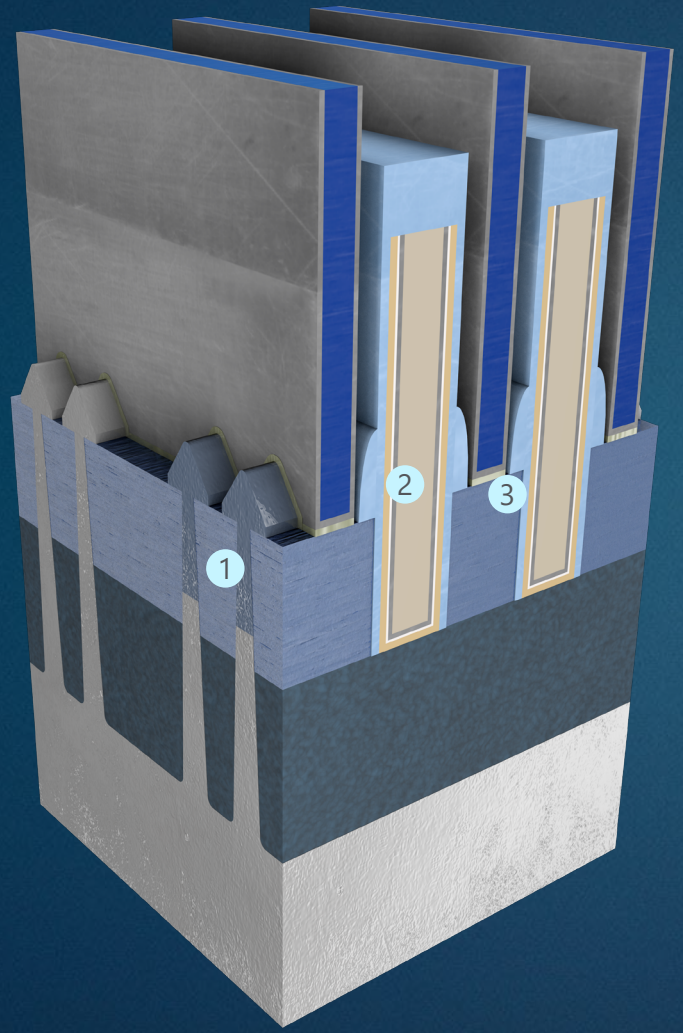
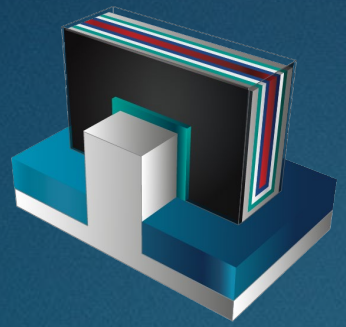
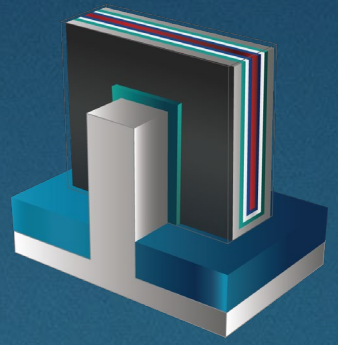
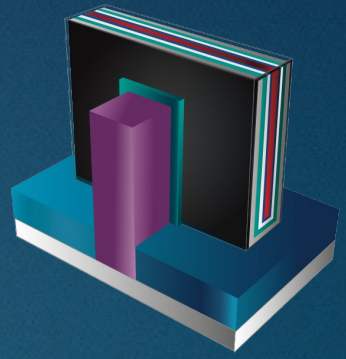
Transistor Scaling Modules and Approaches



Module	Scaling levers
1 Channel and trench isolation	Channel isolation High AR / taller and thinner fins Higher mobility SiGe channel
2 High-k metal gate	T_{ox} scaling V_T tuning – metal gate
3 Transistor source & drain resistance	Source drain engineering (NMOS SiAs, shaping)
New architecture	Gate-All-Around (GAA)

A/R – Aspect Ratio
SDE – Source Drain Extension

Transistor Scaling: Channel and Trench Isolation Module

Inflections		
1st generation FinFET	Scaled tall FinFET	New materials SiGe
		
2012	2017	2020

Scaling lever	High value problems	Solutions
Scaled tall FinFET	Bending of high aspect ratio fins	Co-optimized trench isolation fill Flowable oxide fill, implant treatments, anneals
SiGe pFET	Selective SiGe epitaxy and etching of Si and SiGe fins SiGe fins oxidize during STI	Epi SiGe Plasma nitridation / ALD nitride

PME – Precision Materials Engineering

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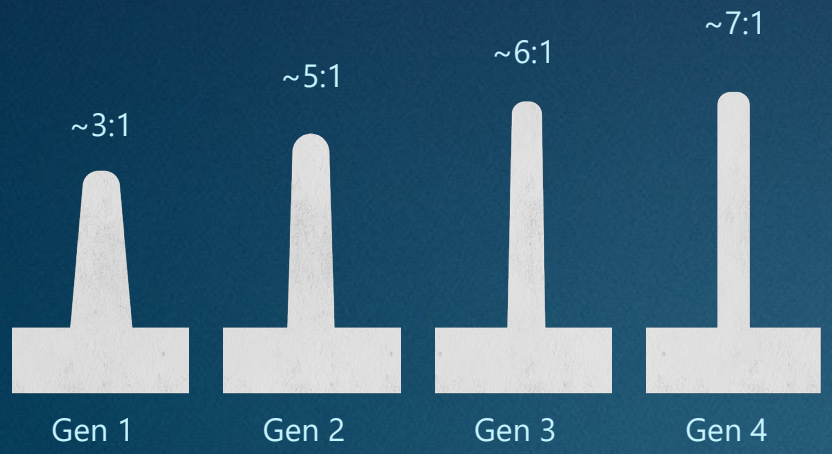
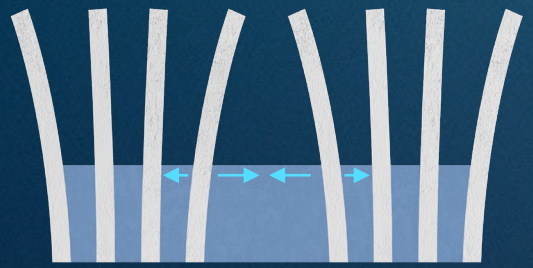
Channel and Trench Isolation Formation

Increasing fin height and aspect ratio

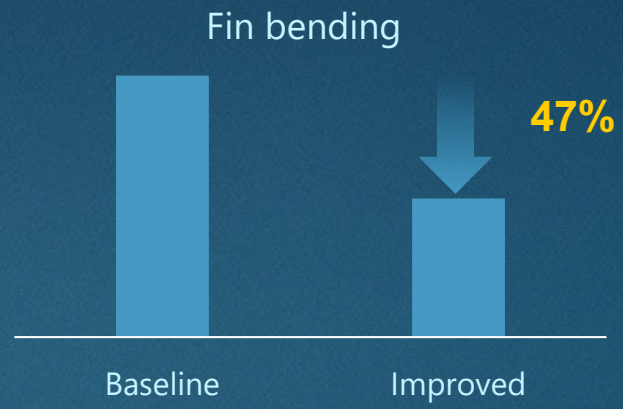


Higher aspect ratio fins have worse fin bending
Bent fins have strain causing μ and V_t changes



$$I_d \approx \left(\frac{H_{fin}}{L_g}\right)\frac{\mu}{t_{ox}}(V_G - V_T)^2$$

Managing fin bending through co-optimized processes



V_T variability ↓ 30%

Drive current I_d ↑ 5%

T.Y. Wen, VLSI 2019

Applied leadership products

Producer® Eterna® flowable CVD oxide and curing for HAR gap fill
VIISta® Trident hot implant precision materials engineering
High speed PROVision® eBeam metrology

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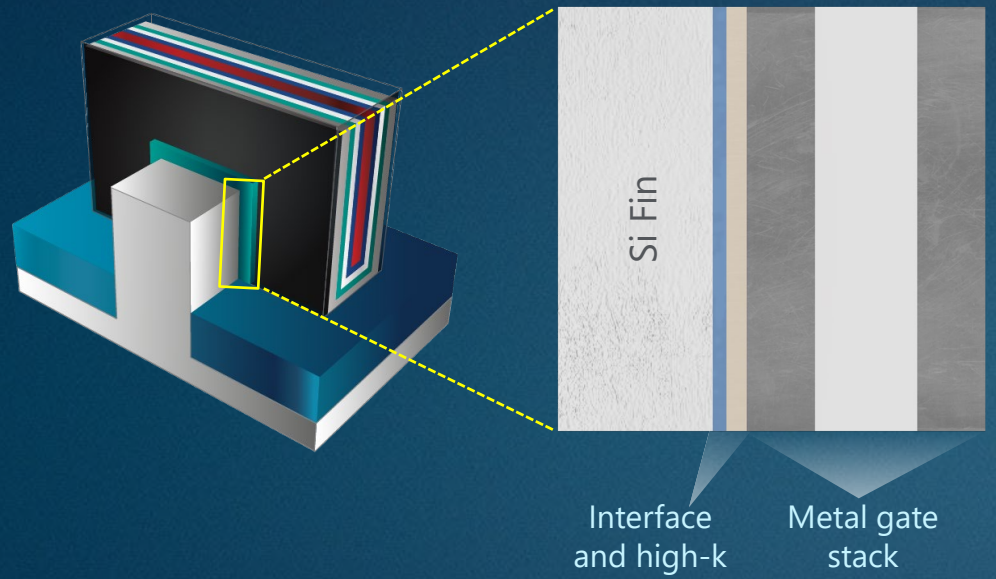
Transistor Scaling: High-k / Metal Gate Module



$$I_d \approx \left(\frac{H_{fin}}{L_g}\right)\frac{\mu}{t_{ox}}(V_G - V_T)^2$$

t_{ox}

Gate oxide scaling
- Interfaces very critical
- How we treat
- How we terminate

t_{ox} scaling boosts I_{on} suppresses I_{off} and improves transistor control

V_T

Metal gate V_T tuning
- Band edge work function
- 6-7 materials stack
- High complexity

Transistor can be tuned for high performance or low power use

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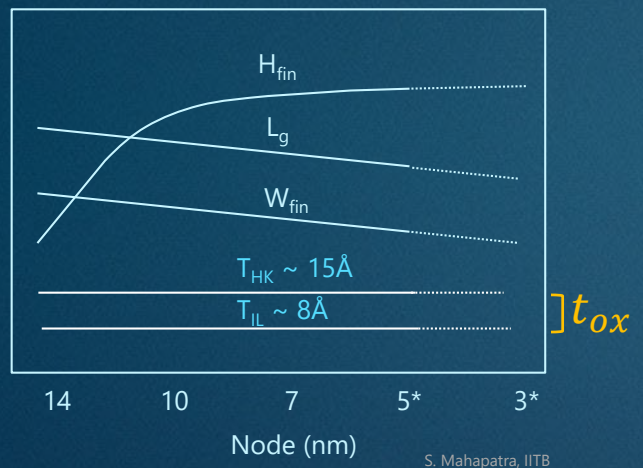
Transistor Gate Oxide Scaling with Co-Optimization

High value problem

Conventional process
Not integrated

Wet chemical oxide
Treatments
ALD High-k

Gate oxide scaling has slowed



S. Mahapatra, IITB

Gate oxide: 8Å interface layer + 15Å HfOx

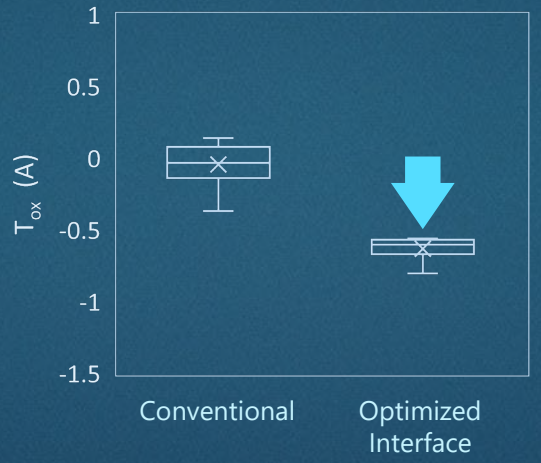
Limited control of interfaces

Solution

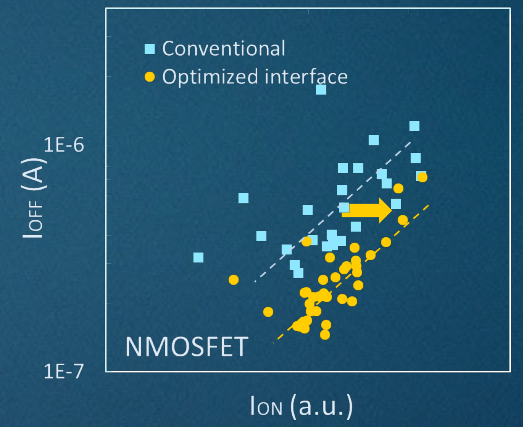
IMS gate stack module
Interface / Materials engineering
Integrated processes

Interface layer
Treatments
ALD High-k

Integration benefits



Drive current



Applied Materials, VLSI 2021

8-10% drive current improvement

Industry's first integrated gate stack solution that re-starts t_{ox} scaling

W_{fin} Fin Width
T_{HK} High-k thickness
T_{IL} Interface layer thickness

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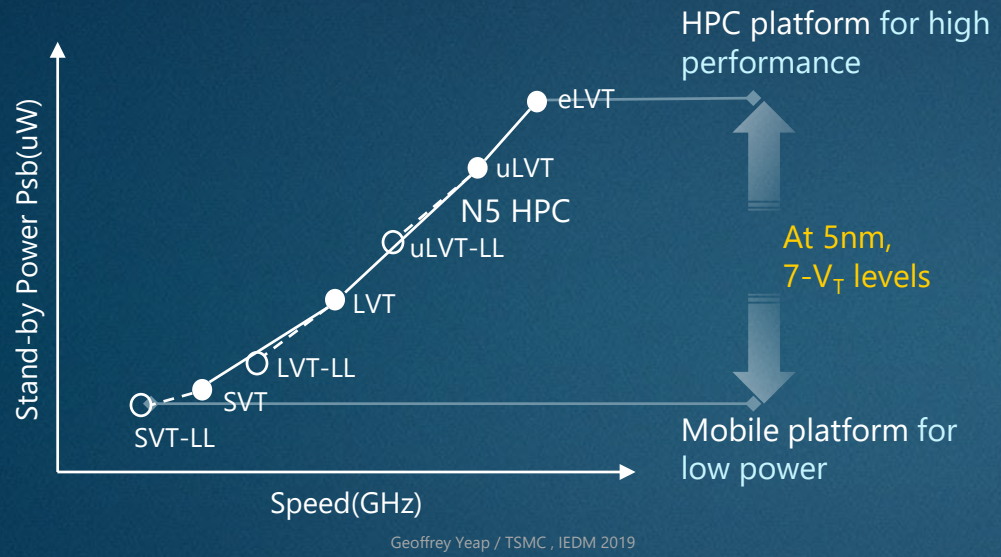
Tuning Transistor Performance with Metal Gate

Multiple V_T flavors for different device types

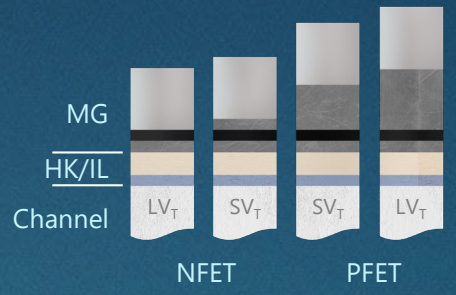


Geoffrey Yeap / TSMC , IEDM 2019

Multiple threshold voltages provides greater design flexibility for a given node, reducing costs

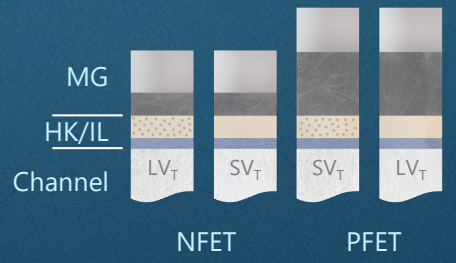
V_T tuning methods

1 Thickness modulation



- ALD work function metal gate layer
- ALD and etch modulate thickness
- As many as 5 materials and 10 layers

2 Dipole engineering



- ALD, anneals and selective Etch
- As many as 3 materials used

HK/IL High-k/ Interface Layer
MG Metal Gate
SV_T Standard Vt
LV_T Low Vt

Applied leadership products

Highly uniform ALD work function metals for Vt engineering control
High vacuum integrated for pristine processing and ambient contamination control

Radiance® rapid thermal processing for precise drive in anneals and densification

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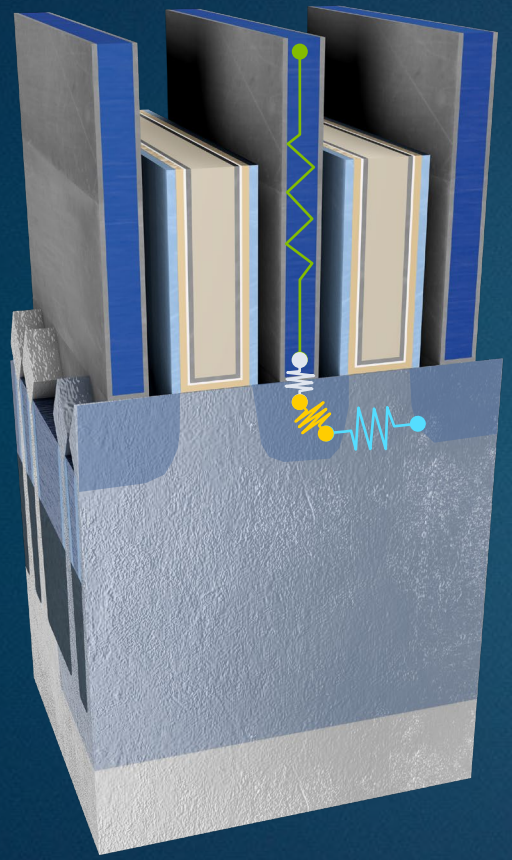
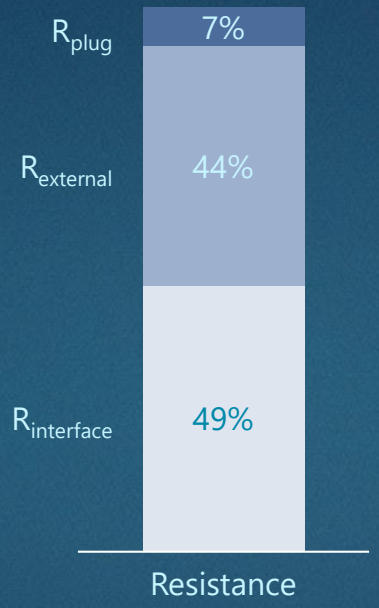
Transistor Scaling: Transistor Resistance

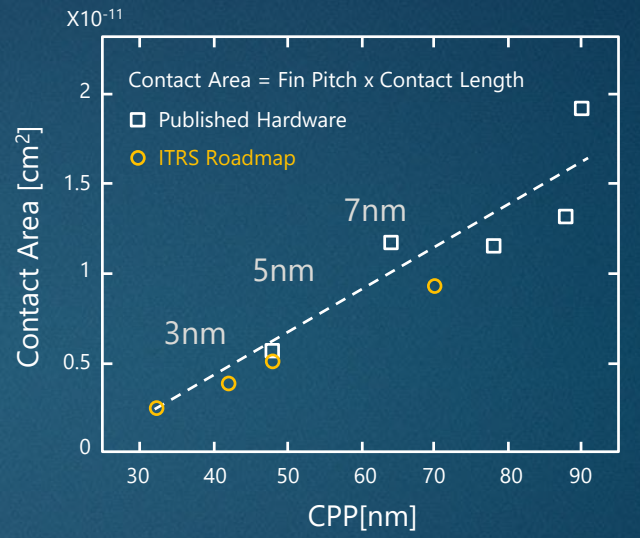
Transistor resistance



Delay $t = \frac{CV}{I_d} = CR$

High value problem





A. Razavieh at el. IEEE 2015

Contact area reduces 25% per node, driving up $R_{interface}$

$R_{interface}$ scaling by epitaxy, implant, metals and anneals co-optimization

$R_{external}$ scaling by sculpting etches, epitaxy, implant and anneal

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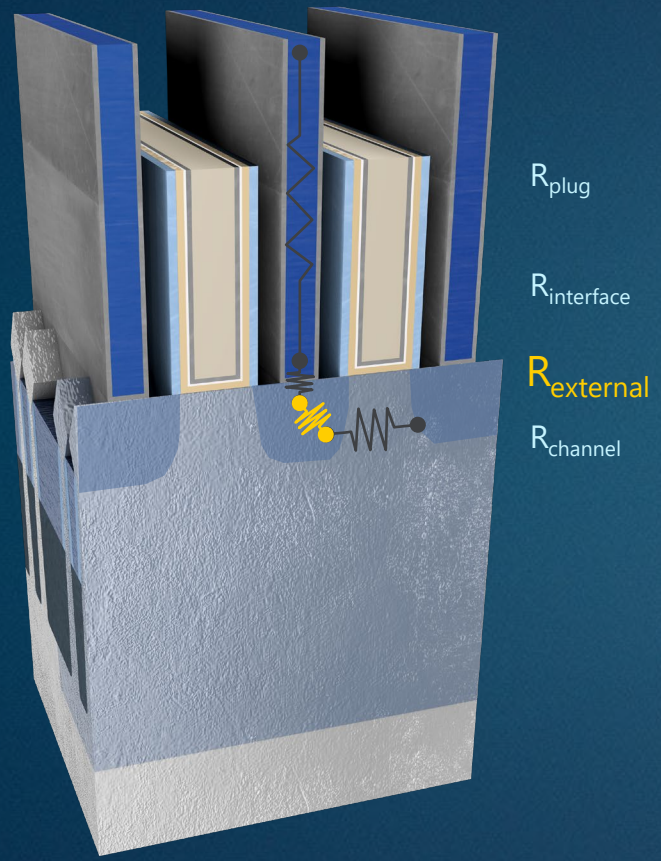
Transistor Scaling: Source/Drain Resistance

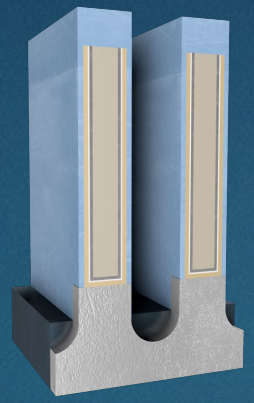
Transistor resistance



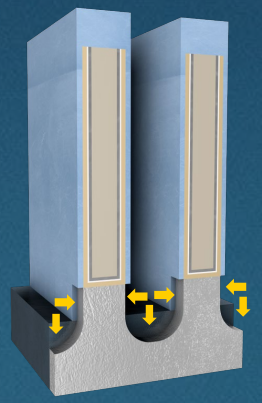
Delay $t = \frac{CV}{I_d} = CR$

High value problem

1 Incoming



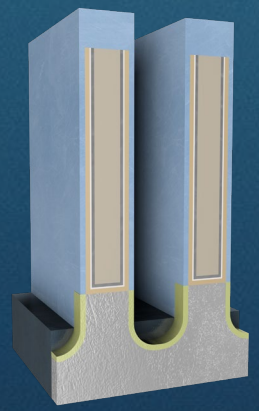
2 Lateral Etch



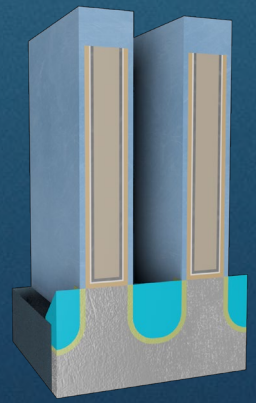
Highly selective lateral etch to avoid spacer loss and optimal cavity profile control

Producer® Siconi™ and Selectra® with >100:1 selective etch

3 Epi SiAs



4 Epi SiP



Co-optimization of lateral etch, epi and anneals demonstrated 8% I_{on} gain

Centura® Prime® Epi with integrated Clarion™ surface preparation for selective SiAs and SiP epitaxy

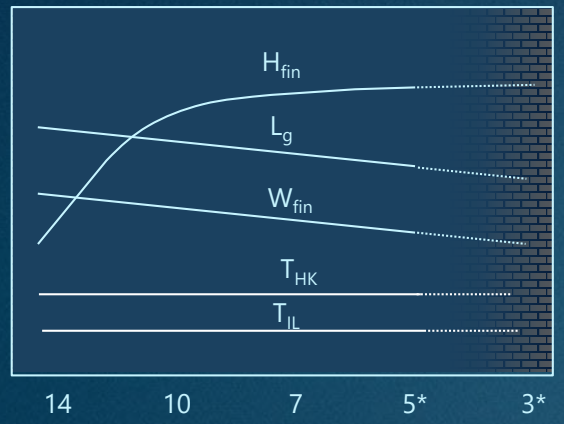
IBM/Applied Materials IEDM 2018

Applied Materials External Use

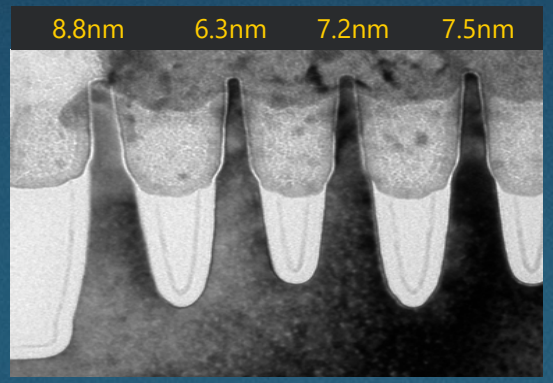
Levers for Logic Scaling: New Architecture

High value problem

Critical FinFET dimensions



Variation in critical dimensions

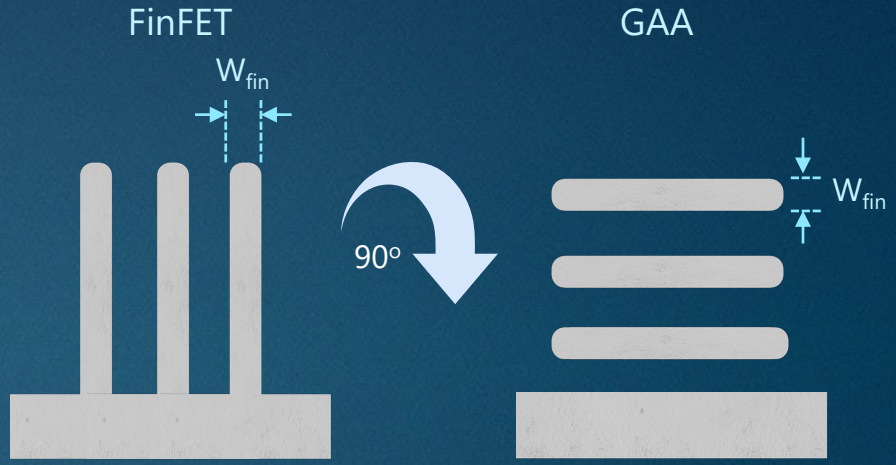


Source: Chipworks

$$I_d \approx \left(\frac{H_{fin}}{L_g}\right)\frac{\mu}{t_{ox}}(V_G - V_T)^2$$

- Fin width defined by litho and etch
- Scaling FinFET below 5nm extremely challenging
- L_g and W_{fin} scaling needed will increase V_T variability

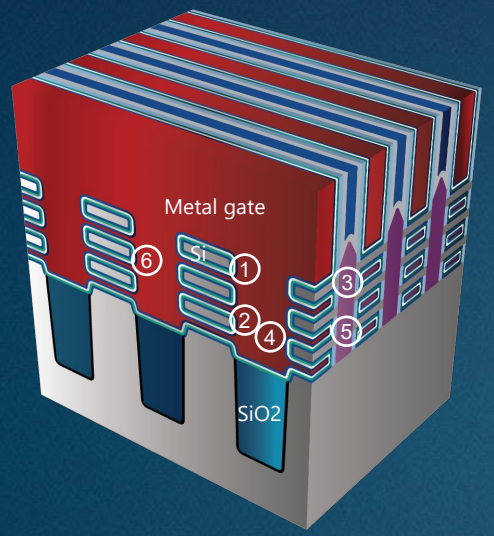
Solution: Gate-All-Around (GAA)



- Channel thickness in GAA is defined using epitaxy and selective etch processes
- Reduced variability & improved channel control

APPLIED MATERIALS

Gate-All-Around: Process Flow



FinFET → GAA (value gains)
↓ leakage/power (geometry)
↑ drive current/speed (stacking)
↑ density (narrower sheet width)
↓ variability (epi defined vs. litho/etch)

↓ 25-30% power; ↑ 10-15% performance#

 # SAFE - Samsung Advanced Foundry Ecosystem, Oct 2020
S/D = Source / Drain

Key new module steps	Requirements
① Super lattice epitaxy	Sharp interfaces, thickness control
② Selective removal	Etch selectivity, no nanosheet collapse
③ S/D stressors (etch, epitaxy)	Controlled recess & growth
④ Inner spacer (sel. removal, dep)	Controlled lateral recess, gapfill
⑤ Metal gate between nanosheets	New materials + void-free gapfill
⑥ Super lattice metrology	Buried defect detection, measurement

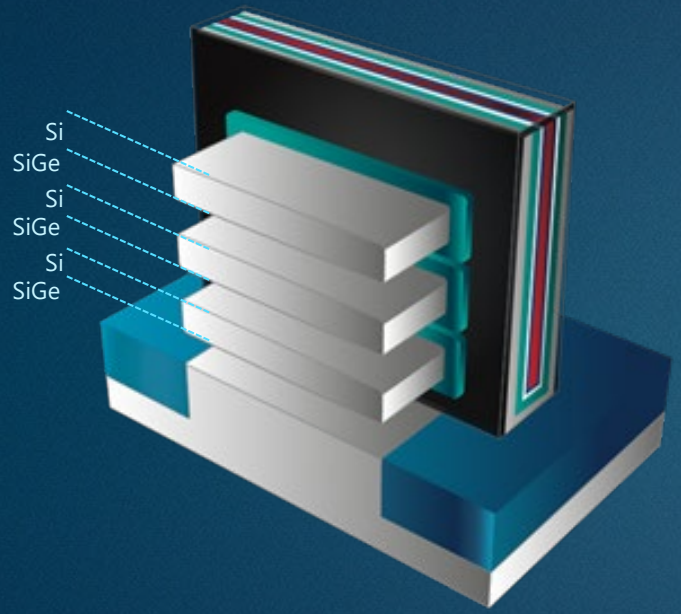
Critical steps defined by materials and process engineering

Applied Materials External Use

APPLIED MATERIALS

Gate-All-Around: Superlattice Epitaxy and Removal

High value problem

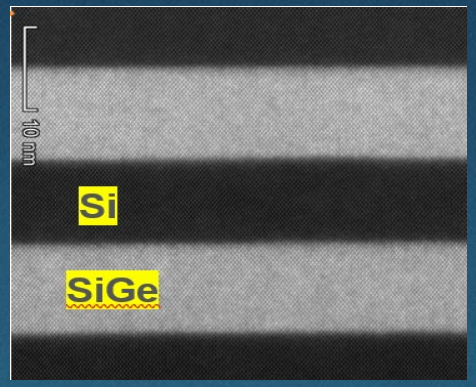


Good thickness uniformity

Abrupt SiGe/Si profile

Highly selective SiGe removal

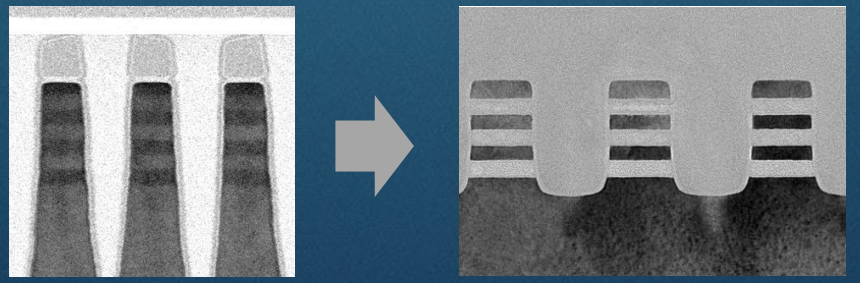
① Si/SiGe superlattice formation



Optimized process for Si/SiGe interface and stack uniformity

Centura® Prime® Epi SiGe /Si epitaxy

② Si channel release



Pattern etch

Selective SiGe removal

SiGe:Si removal selectivity of >500:1
Optimal edge profile maintained

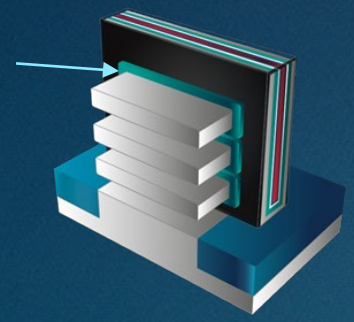
Producer® Selectra® selective etch

Applied Materials External Use

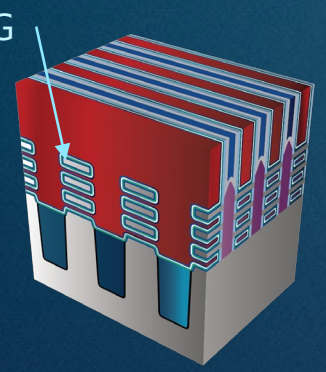
APPLIED MATERIALS®

Gate-All-Around: HKMG & Inner Spacer Modules

High value problem

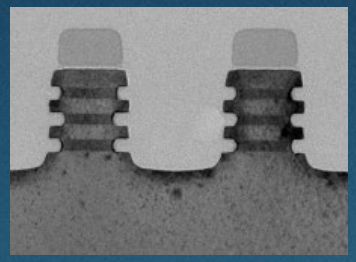


Uniform SiGe lateral push amount
High SiGe to Si selectivity

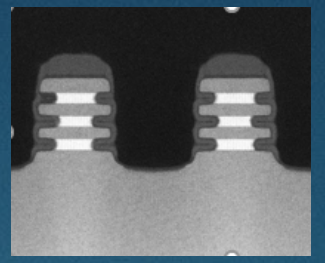


Narrow GAA channels require advanced conformality-underside of channel “slabs”

④ Inner spacer formation



Selective SiGe removal



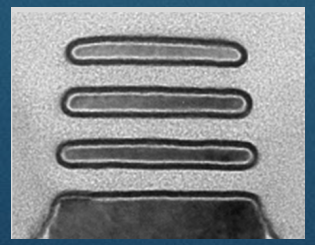
ALD spacer deposition

Tunable SiGe : Si selectivity for best-in-class recess uniformity

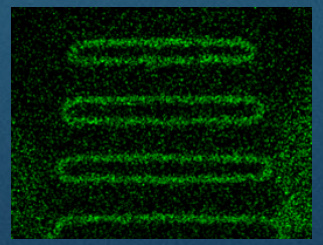
ALD spacer deposition

Producer® Selectra® selective etch

⑤ High-k and metal gate module



IL and ALD high-k



N atom concentration

IMS gate stack module
ALD work function metals

ALD metal gate
Radiance® RTP thermal treatments
Centura® DPN plasma treatments

Applied Materials External Use

APPLIED MATERIALS®
make possible

PART 2

Logic Contact and Interconnect Challenges and Roadmaps

Mehul Naik, Ph.D.
Managing Director
Semiconductor Products Group

LOGIC MASTER CLASS | June 16, 2021

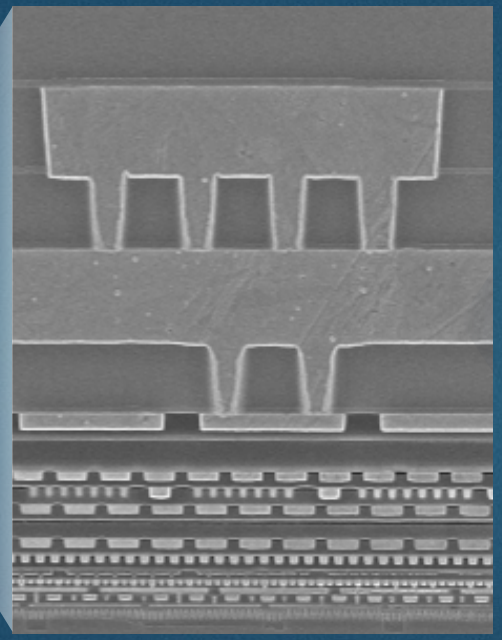
Applied Materials External Use

Zooming in on Smartphone Chip Interconnects

Source: Apple

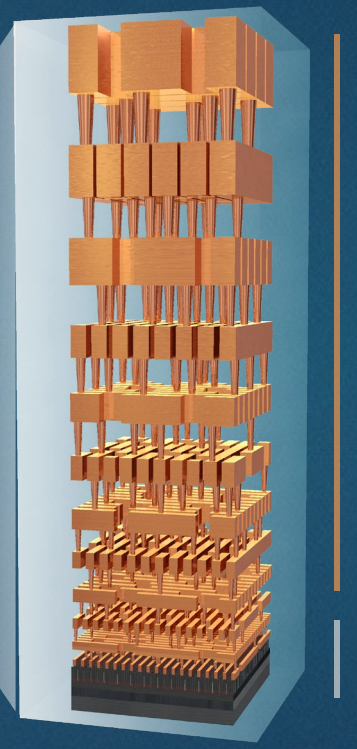
Source: Apple

Processor chip: 88mm^2 size
8.57 mm x 10.23 mm



Source: TechInsights

Microscope cross section view of chip



3D model of a chip

>15 layers
stacked copper interconnects

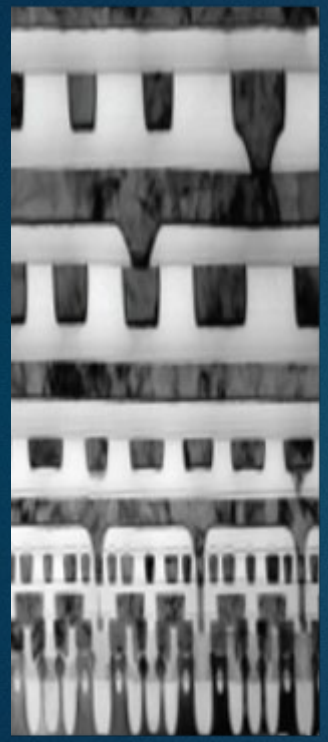
>24 billion
contact trench and via connections

>11.8 billion
transistors

APPLIED MATERIALS®

Scaling Implication on Interconnect Performance

CMOS device components

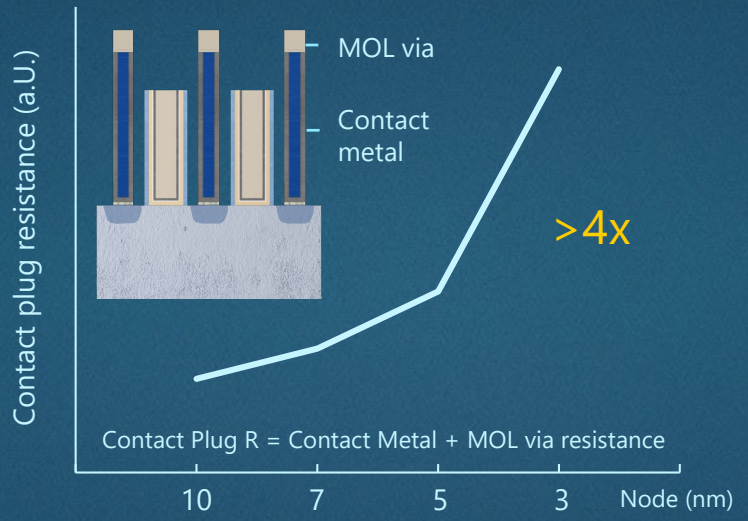


Source: TechInsights

Contacts
Connect transistors to the rest of the chip

Interconnect
Carry current and connect discrete transistors

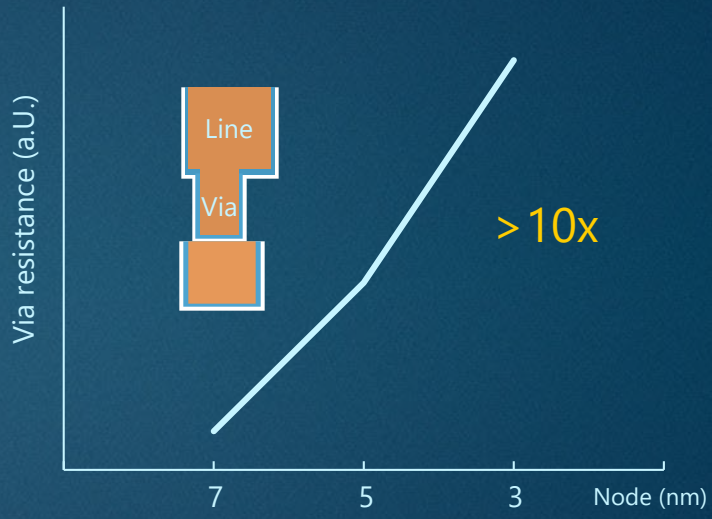
Contact plug resistance
Reduces drive current



>4X increase in contact plug resistance
7-10% of transistor resistance from contact

Applied Materials Model

Interconnect via resistance
Increases dynamic power dissipation

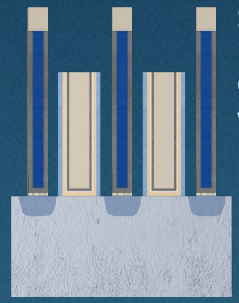
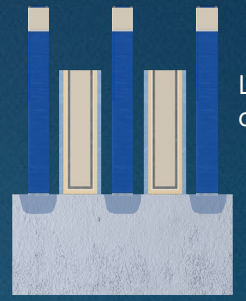
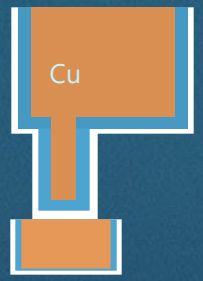
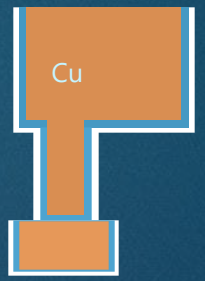
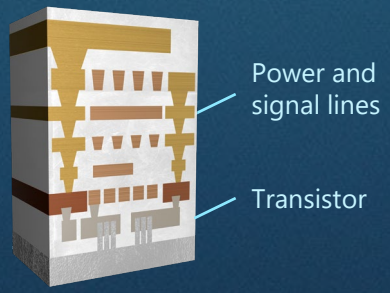
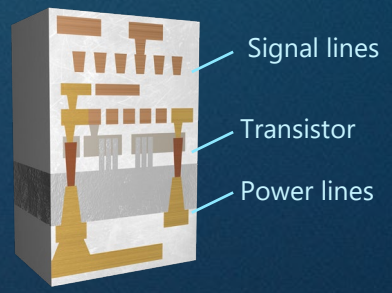


>10X increase in via resistance
> **1/3rd** of chip power is consumed in Interconnect

Applied Materials Model

APPLIED MATERIALS

Scaling of Contact and Interconnect

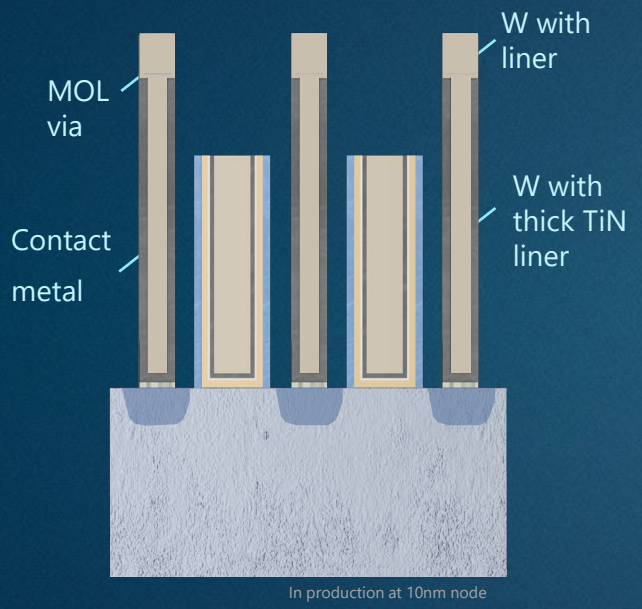
Scaling challenge	Key modules	State-of-the-art	Inflections
Transistor resistance reduction	Contact Middle of line (MOL)		
RC delay and power consumption reduction	Interconnect (Line, via, dielectric)		
New ways to shrink	Buried Power Rail Backside Power Delivery		

Applied Materials External Use

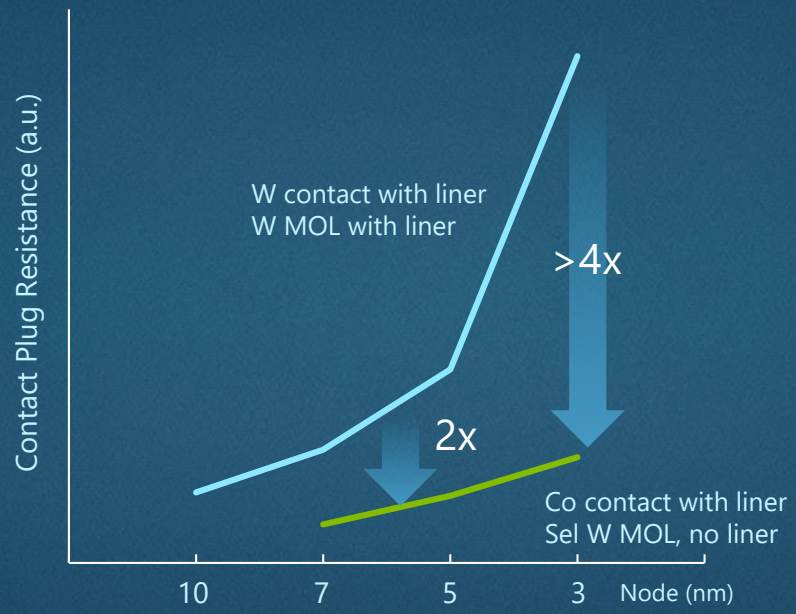
APPLIED MATERIALS

Contact: Innovations Enable Metal Fill Without Liners

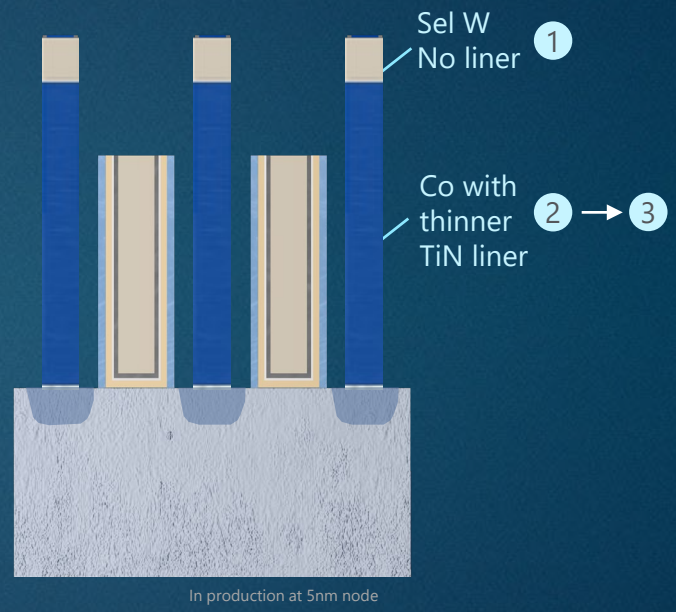
CD shrink + liner = high R, r_c



Contact resistance throttles transistor performance



Thinner/ no liner & low R metal for improved performance & yield



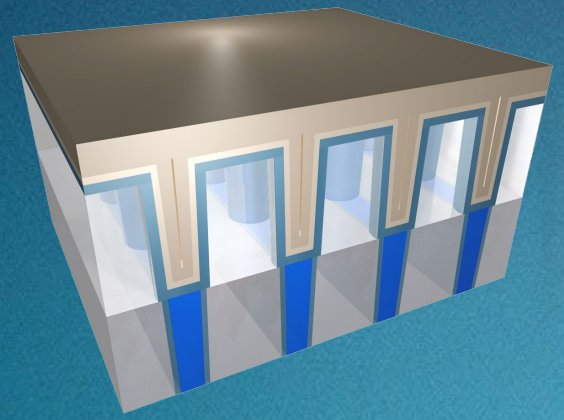
1. Endura® Volta® Selective W CVD
2. Endura® Volta® Cobalt CVD
3. Next-generation liner-less metals at n+1

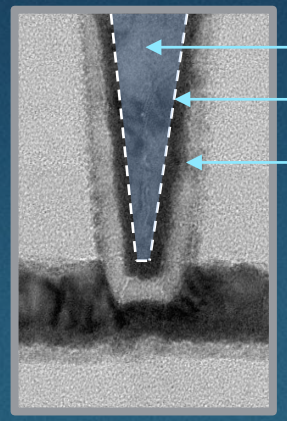
Applied's low R solutions enable **>4X** reduction in contact plug resistance

Applied Materials External Use

Selective W Contacts Delivers Lower Power

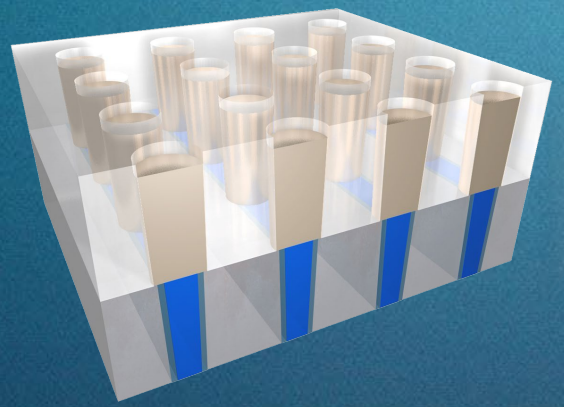
Conventional Approach

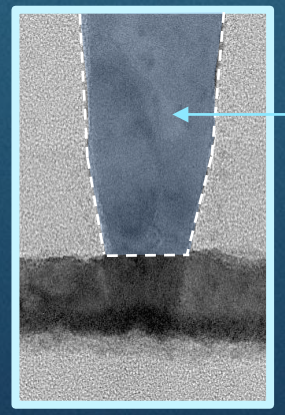




75% of volume consumed by high resistance materials

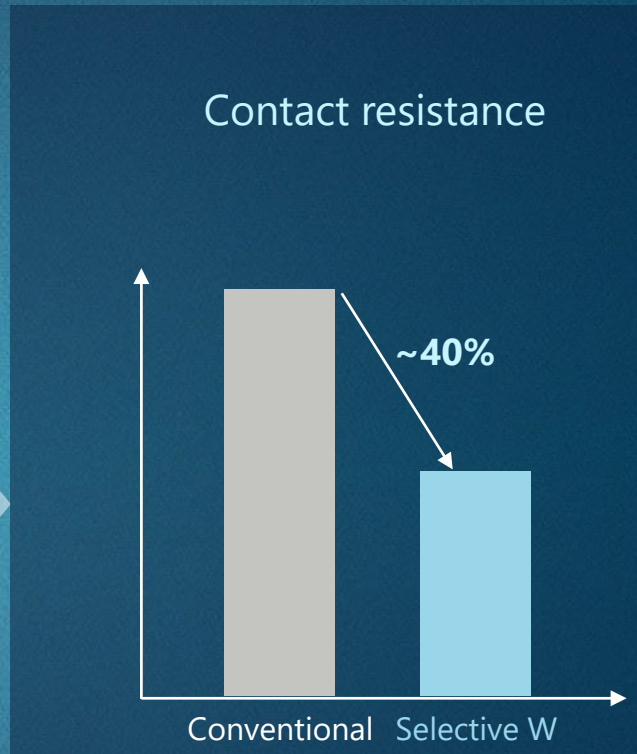
Endura® Volta® Selective W





No extra liners or nucleation layers
100% conductance

Applied Materials Data

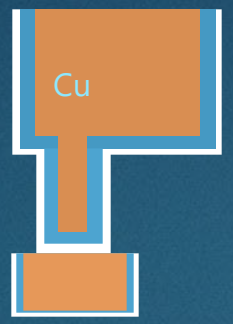
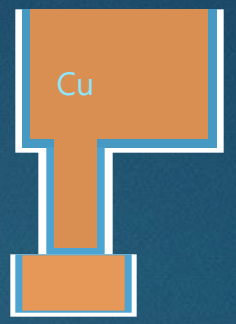


At fixed frequency
6% lower power

Applied Materials Data

APPLIED MATERIALS®

Levers for Interconnect Scaling

Scaling challenge	State-of-the-art	Inflections
RC delay and power consumption reduction	Copper with conformal ALD barrier 	Copper with selective ALD barrier  Higher modulus low-k films

Contributing factors	High value problems	Solutions
Interconnect (Via) Interconnect (Line)	High interconnect resistance increases power dissipation & slows down devices	Selective ALD barrier Thinner liner with advanced Cu reflow
Dielectric	Pattern integrity at tightest pitch	High modulus low-k at tightest pitch

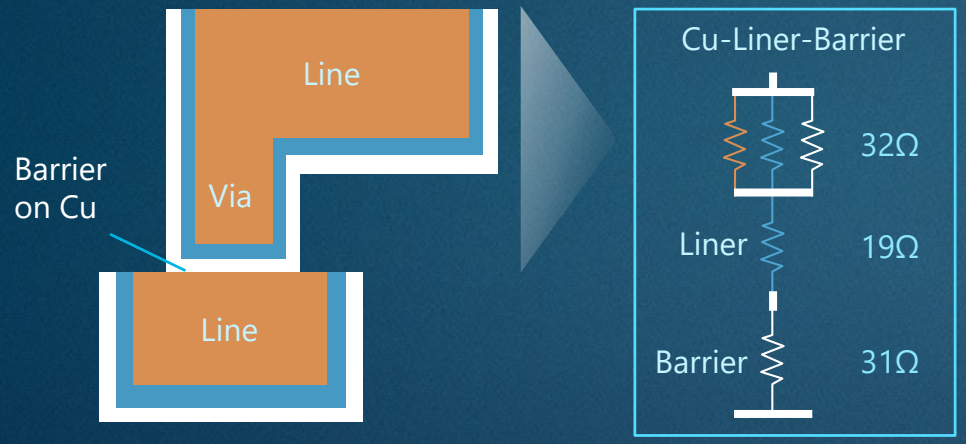
Applied Materials External Use

APPLIED MATERIALS

Interconnect Via Resistance Scaling Solutions

High value problem

Conventional: low conductivity interface layers

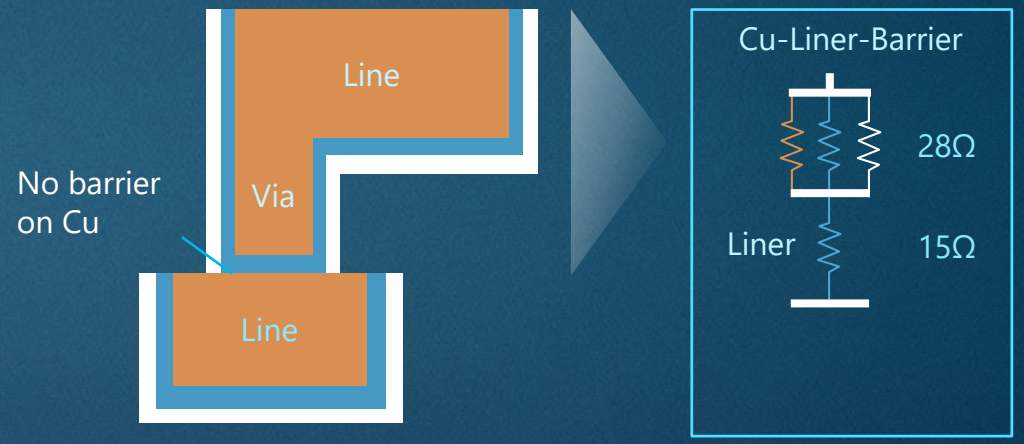


High via resistance, RC delay & dynamic power loss

Liner: Cobalt
Barrier: Tantalum Nitride

Solution

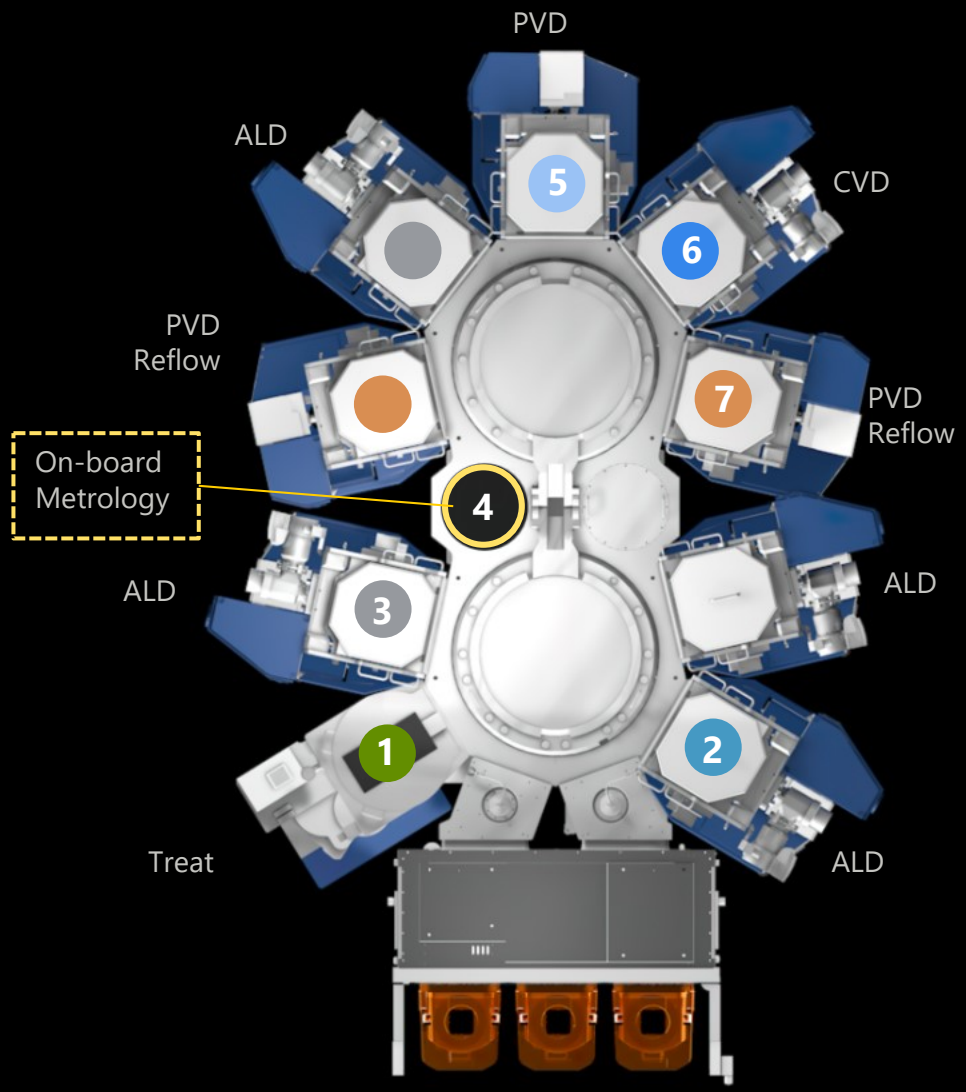
Selective ALD barrier: deposit on dielectric and not on Cu

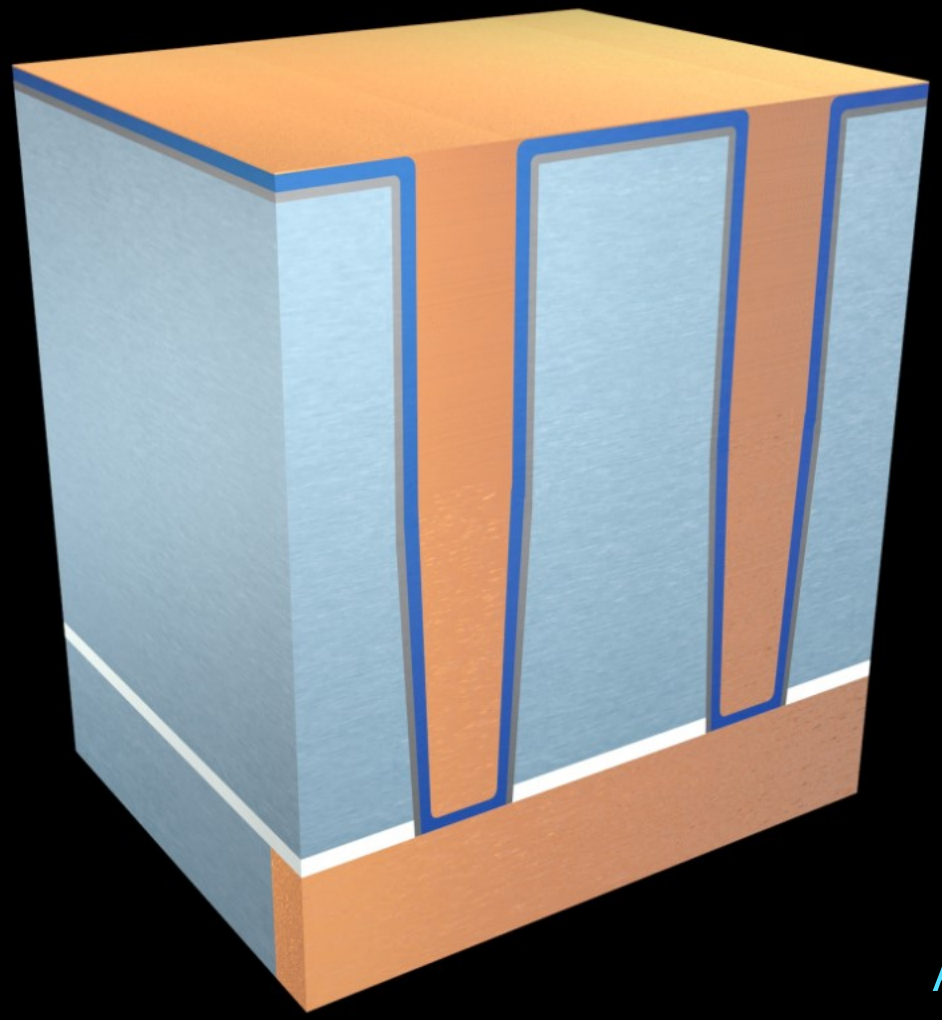


~ 47% improvement in via resistance

Applied Materials Data

APPLIED MATERIALS





INTEGRATED SOLUTIONS

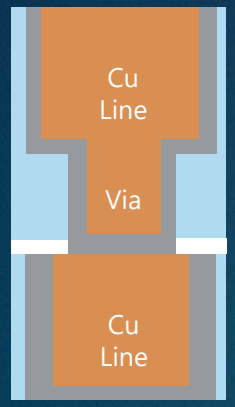
7. Copper Reflow
6. Liner Deposition
5. Material Modification Treatment
4. Integrated On-Board Metrology
3. Selective ALD Deposition
2. Interface Engineering
1. Surface Preparation

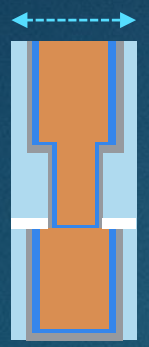
All 7 steps in vacuum unique to Applied

Applied Materials External Use

Applied's Unique Solution Lowers Interconnect Resistance

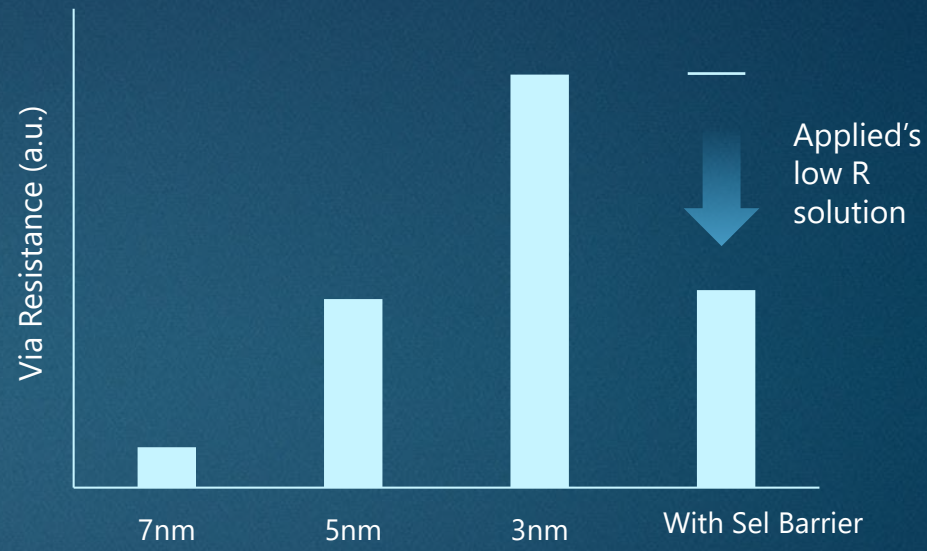
Then		Now	
60nm	→	15nm	critical width
3		7	# process steps
2		4	# materials
conventional		selective	processes
bulk films		interfaces	properties
plating		reflow	narrow wire fill





1/2000th human hair

Selective barrier process



~50% ↓ via R	*	>1B vias	*	5 critical levels	=	scaled power savings
(single via)		(via per layer)		(# of layers)		(net gains)

Applied Materials Data

Applied Materials External Use

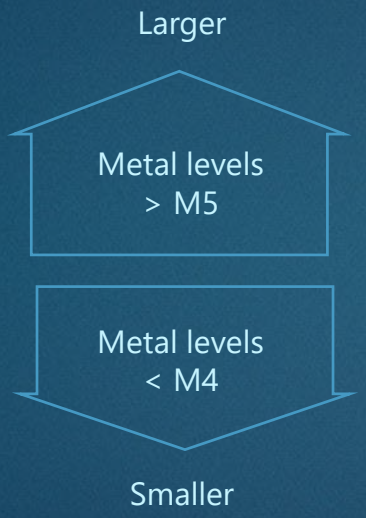
APPLIED MATERIALS

Dielectric Solutions to Sustain Capacitance Scaling

High value problem

Low-k pattern integrity for small features

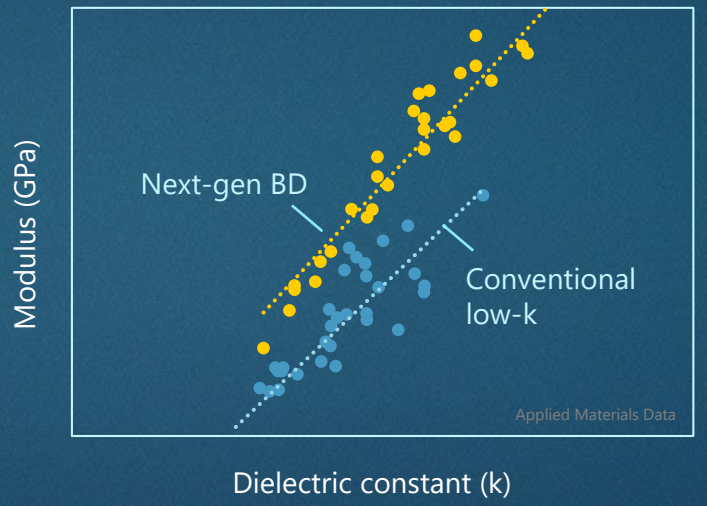
Source: TechInsights



At smaller pitch, low mechanical strength leads to pattern collapse

Solution

Next-gen Black Diamond® (BD) films: higher mechanical strength



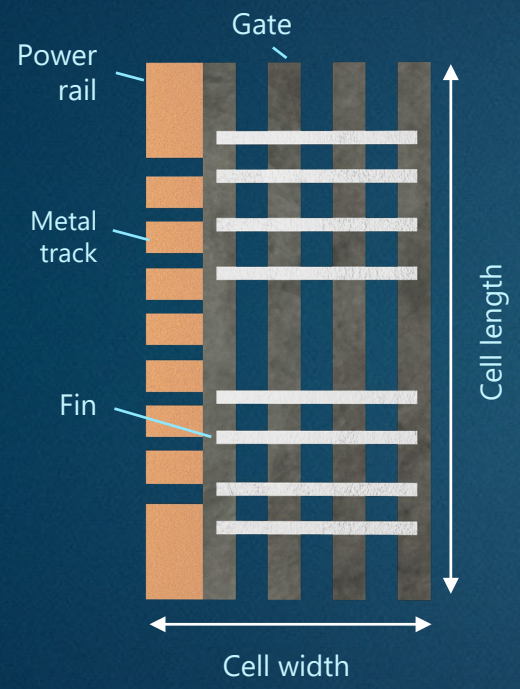
Up to 40% higher modulus at the same dielectric constant

Higher strength films ensures pattern integrity for narrow structures

APPLIED MATERIALS®

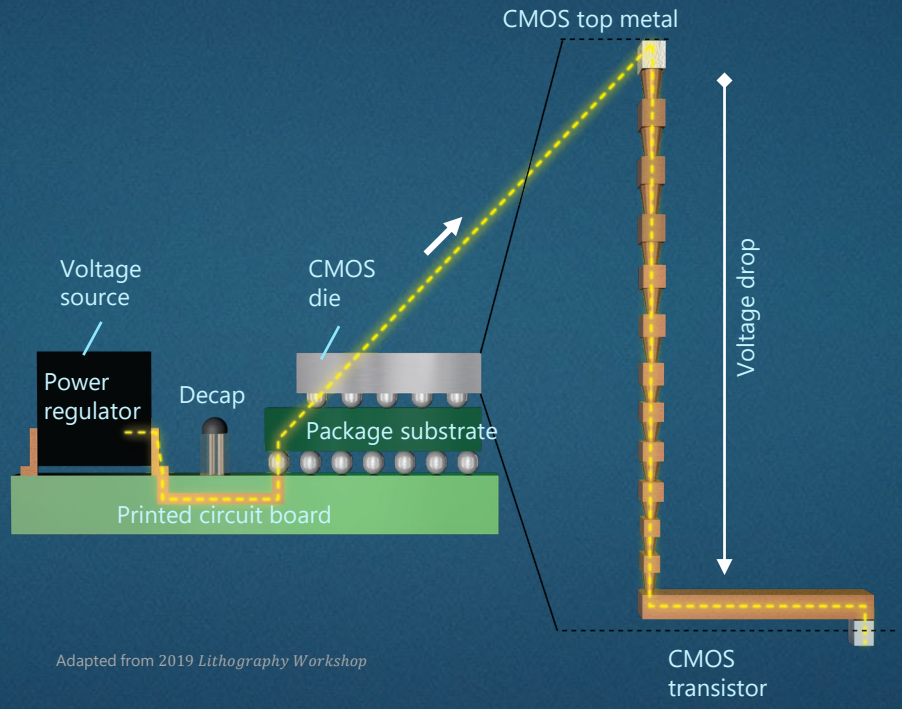
PPACt™ Limitations of Power Delivery Architecture

Cell **area** scaling challenges



Power rail CD ~ 3x min CD

Power delivery losses (voltage drop)



Adapted from 2019 *Lithography Workshop*

Target drop margin is ~10% in power delivery network

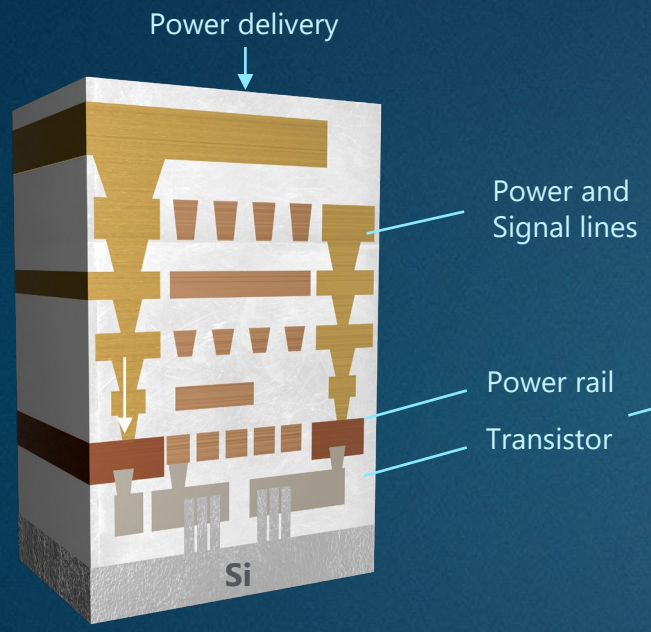
Large drop from 12+ levels due to metal resistance

Excessive drop (~50%) prevents scaling @ edge

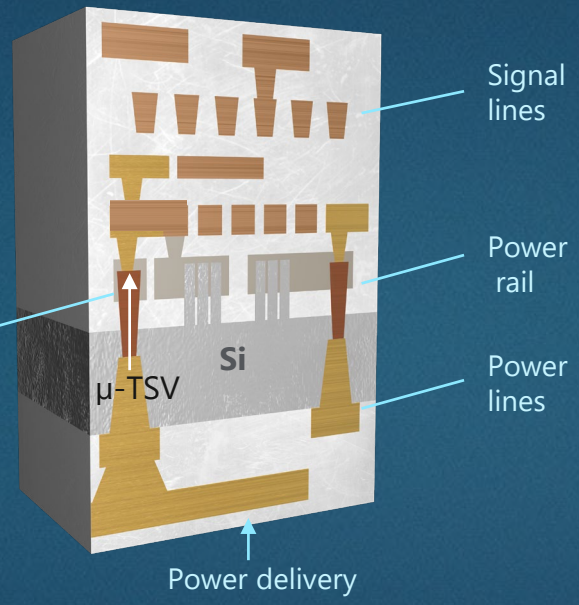
APPLIED MATERIALS

Power Rail Inflection: Backside Power Delivery

Conventional



Buried power rail with backside PDN



Key changes:

1. Separation of power and signal lines
2. Power rails and power lines embedded in the silicon substrate
3. Power delivery from the backside

PDN Power Delivery Network

PPACt Benefits

1.7 to 7x
Voltage reduction

20 to 33%
cell area reduction

Unit Process Leadership

High AR power rail fill
Pre-clean for low R_c
µ-TSV etch
µ-TSV isolation
µ-TSV Cu metallization
Metal CMP

Applied Materials External Use

APPLIED MATERIALS

APPLIED MATERIALS®
make possible

PART 2

Logic Patterning and DTCO Challenges and Roadmaps

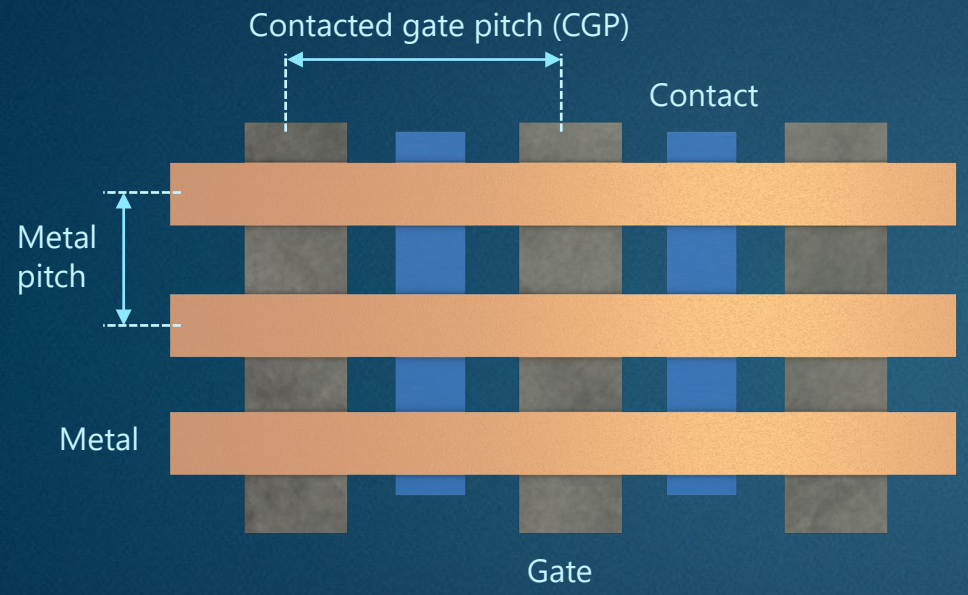
Regina Freed
Managing Director
Semiconductor Products Group

LOGIC MASTER CLASS | June 16, 2021

Applied Materials External Use

Two Approaches Enable Logic Cell Area Reduction

Critical parameters in transistor density scaling



Simple logic unit cell:

Size = Metal pitch * CGP

1 Traditional scaling via pitch reduction

Shrink every feature uniformly

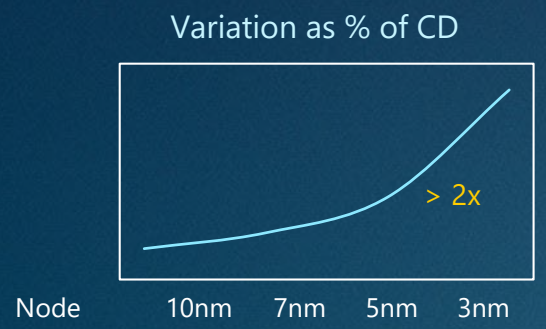
2 Design and Technology Co-Optimization (DTCO)

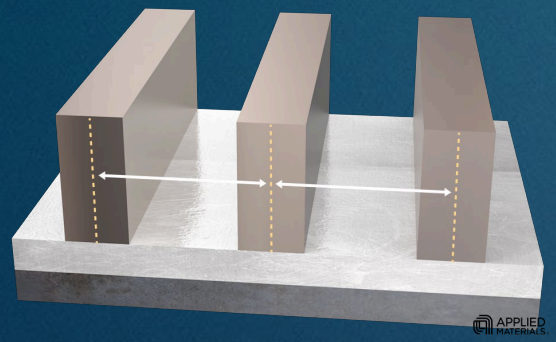
Shrink using a combination of architectures, processes and materials

Applied Materials External Use

Logic Pitch Scaling Challenges

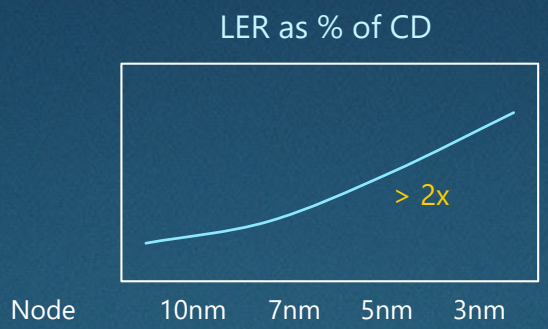
Size variation across features

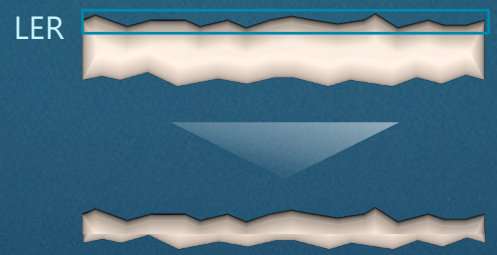




Variation increasing in local and across-wafer CDU

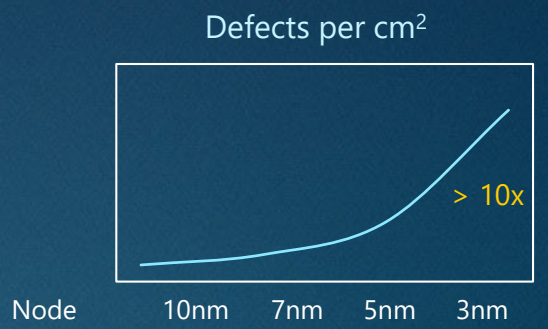
Variation within a feature

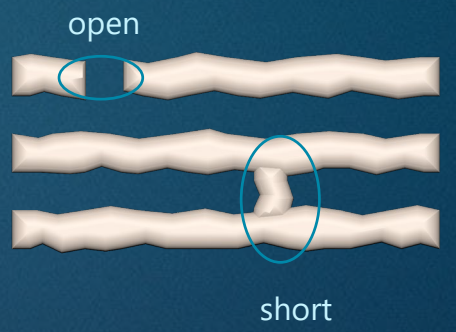




Line edge roughness approaching 30% of line width

Stochastic defects





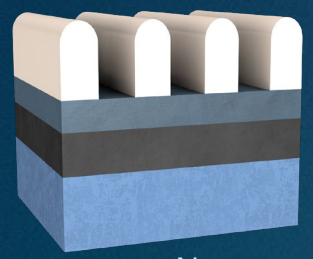
Drastic rise of stochastic pattern defects – opens and shorts

CDU = Critical Dimension Uniformity
LER = Line Edge Roughness

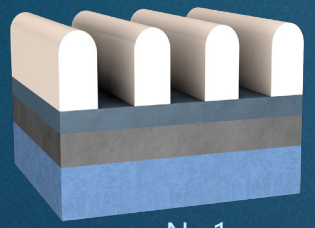
Applied Materials External Use

Innovations to Enable Low Variability EUV Etch Process

Higher selectivity CVD hardmask



N



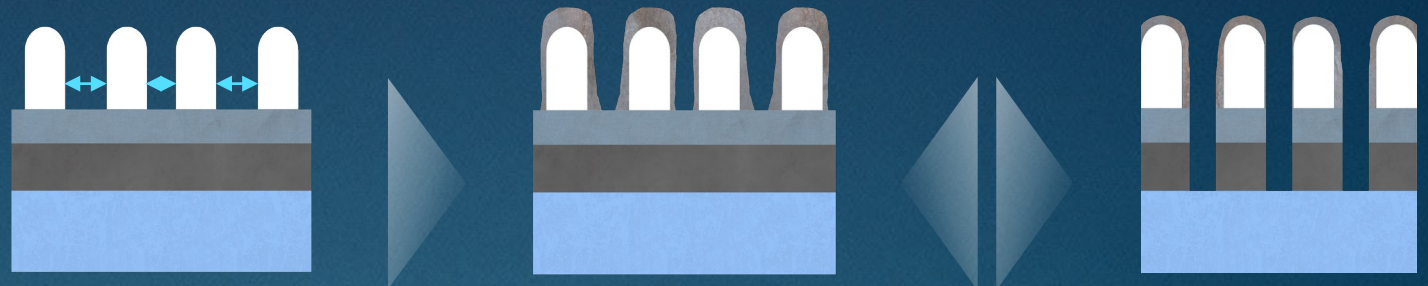
N+1

Key challenges:
Material composition, resist adhesion and etch transfer

Industry leading CVD films for reduced roughness and high etch selectivity

+

Advanced etch and deposition capability

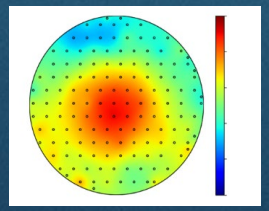


In-situ deposition with advanced pulsing for better profile and CD uniformity

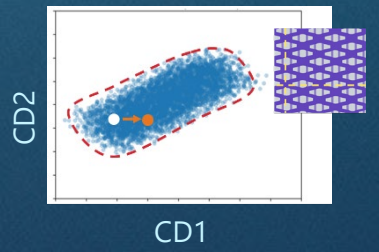
+

Unique metrology for faster and better sampling accuracy

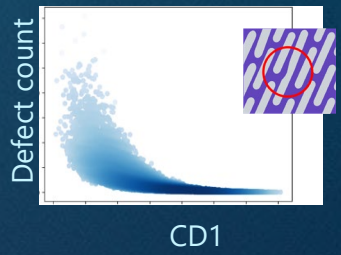
Spatial signatures



Process tradeoffs



Defect windows

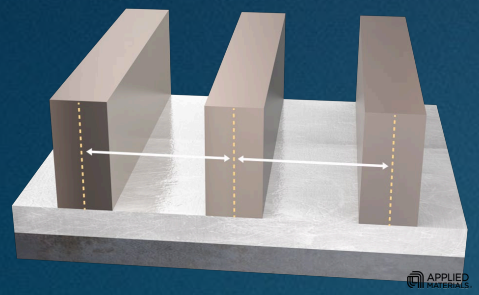


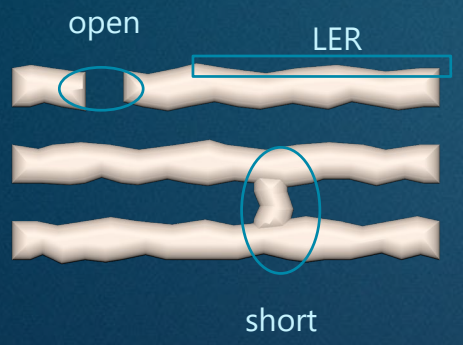
Non-destructive variation measurements with actionable insights AI[x™]

Applied Materials External Use

Patterning Defect Reduction with Co-Optimization

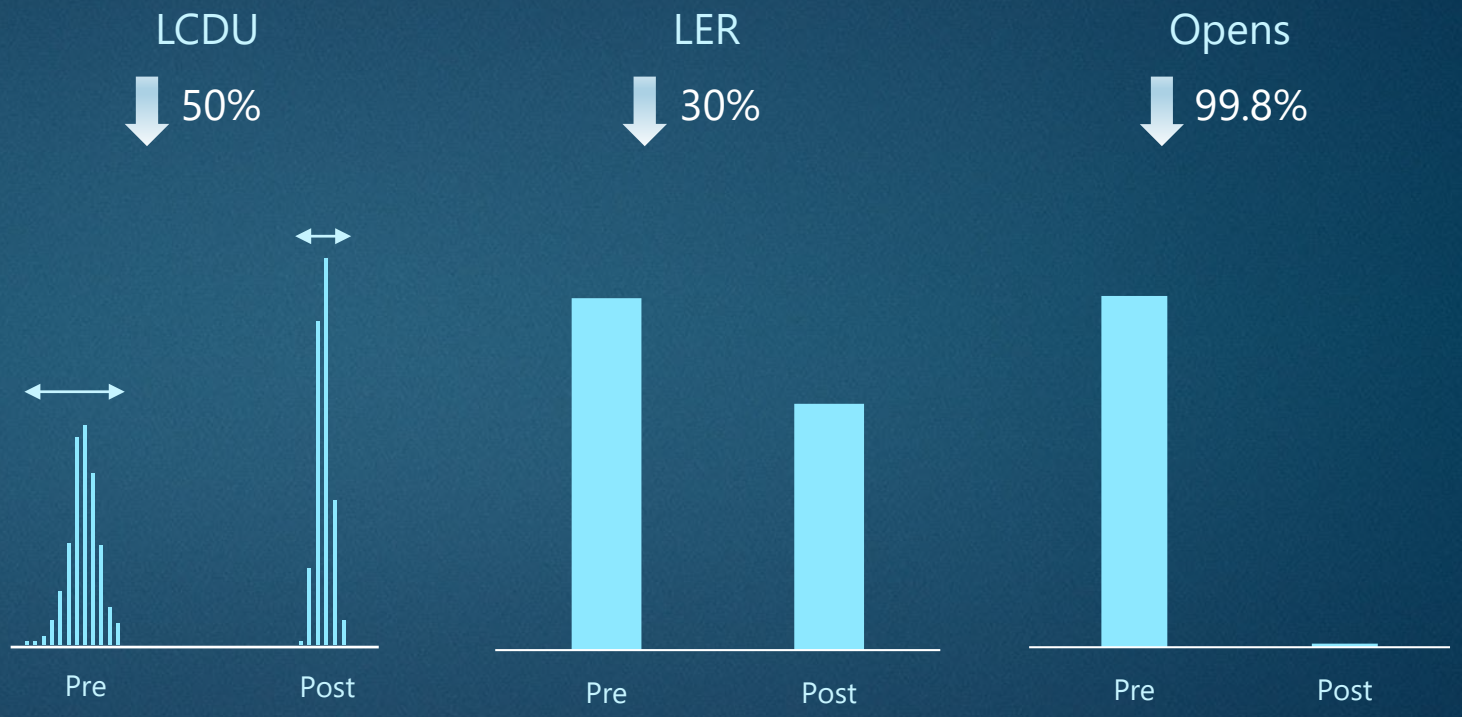
Key challenges in EUV patterning





Local and across-wafer CD uniformity
Line Edge Roughness
No pattern defects (shorts, opens)

Enabling improved CD uniformity and defect performance



Co-optimized dep-etch processes with integrated metrology significantly reduce defects

LCDU = Local CD Uniformity

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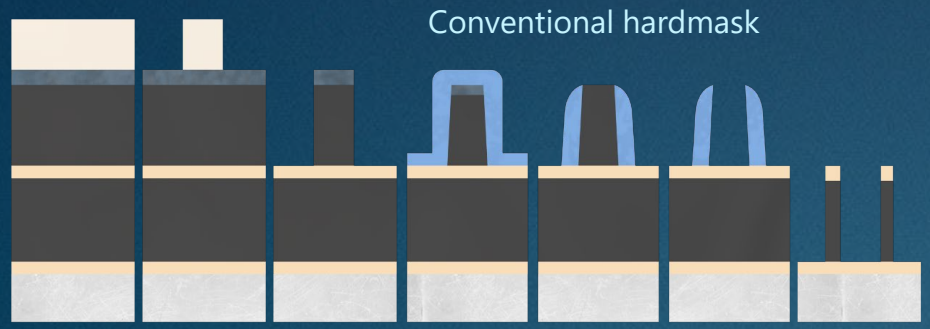
Cost-Effective and Reduced Variability Patterning Solution



	Conventional EUV SADP	New materials with co-optimization
Patterning films	Spin-on and furnace	High quality CVD films – DARC®, APF®
# of layers	5	3
Co-optimization	Required	CVD co-optimized with Sym3® etch
Pattern variability	High	Low

New innovative materials and co-optimization lead to improved uniformity and 30%↓ Steps

EUV = Extreme ultra-violet lithography
SADP = Self-aligned dual patterning

Applied Materials External Use

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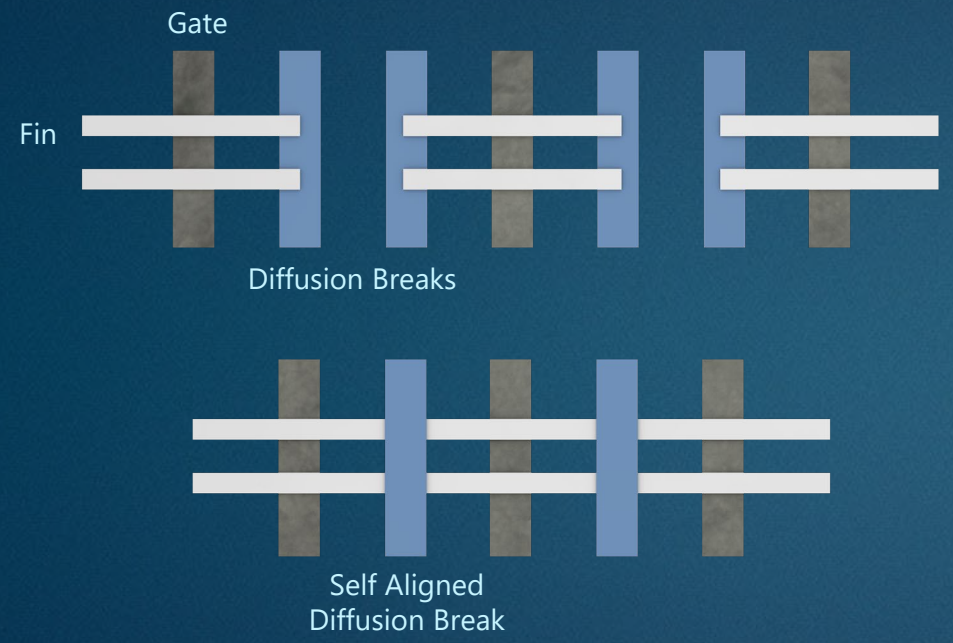
DTCO Enabled by Materials Engineering Portfolio

Example of DTCO: Self Aligned Diffusion Break

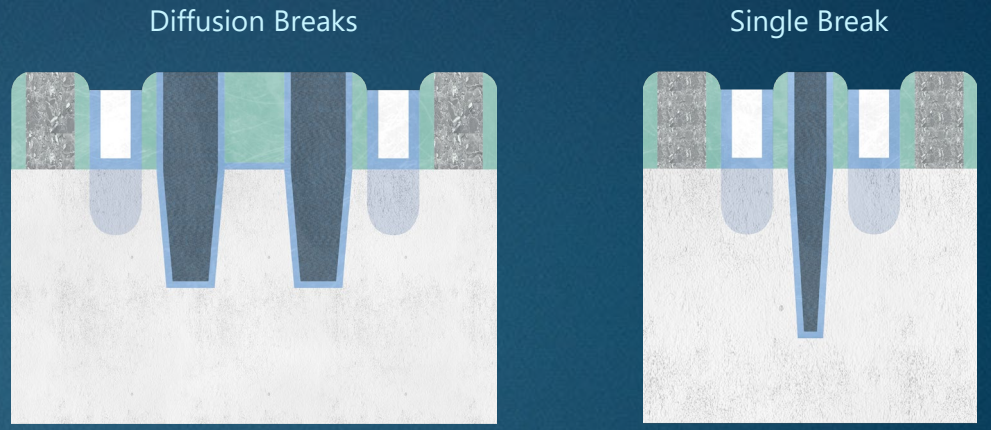


15% horizontal scaling by reducing the CGP grid

Requirement: high quality oxide material to isolate transistors

CGP = Contacted Gate Pitch
FCVD = Flowable CVD
CMP = Chemical Mechanical Planarization

Scaling the Diffusion Break



High aspect ratio, small width

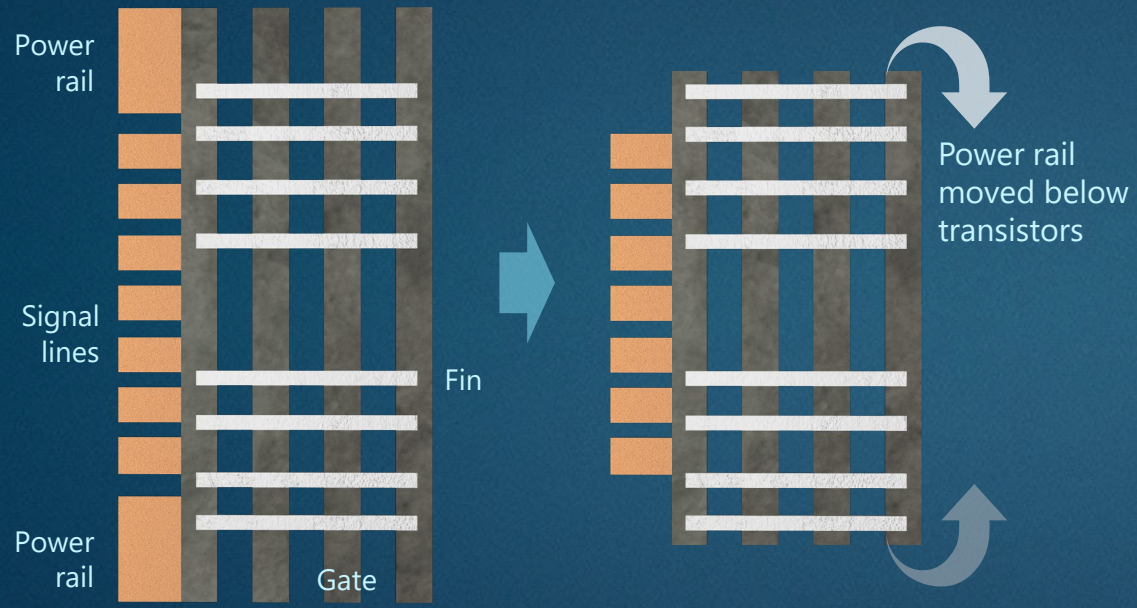
Enabled by Producer® Eterna® FCVD™ and Reflexion® LK CMP

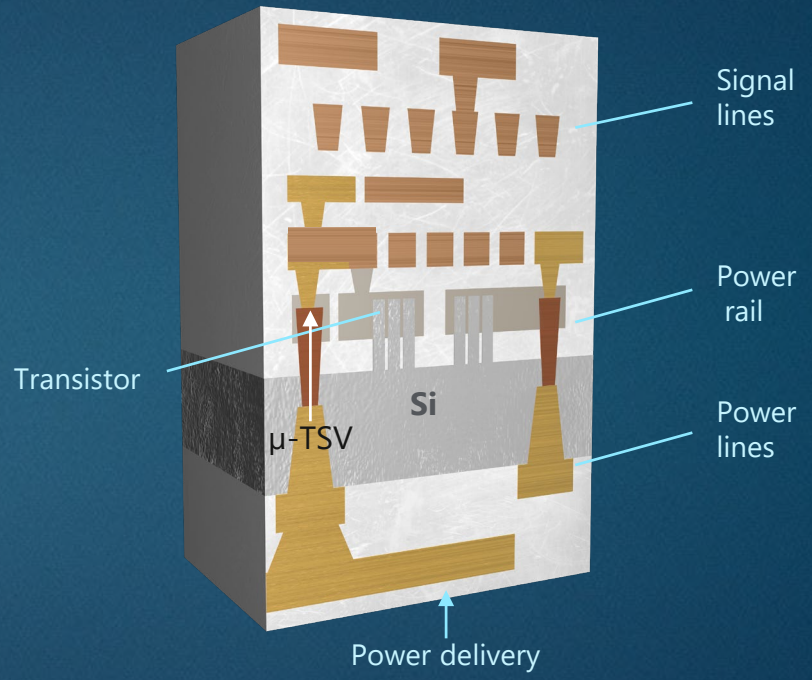
Applied Materials External Use

APPLIED MATERIALS®

Future DTCO Modules for Logic Scaling

Buried power rail with backside PDN





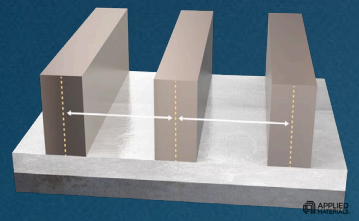
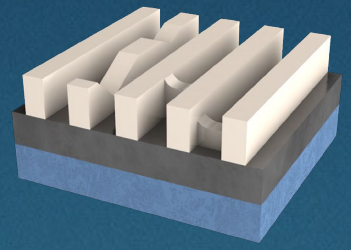
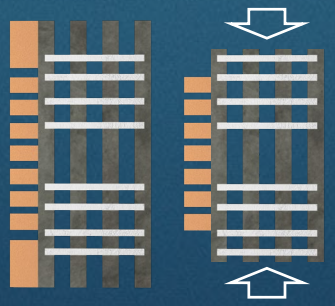
20 to 33% cell area reduction with benefit of performance gains
Enabled by architectures, processes and materials

Applied Materials External Use

• PDN Power Delivery Network

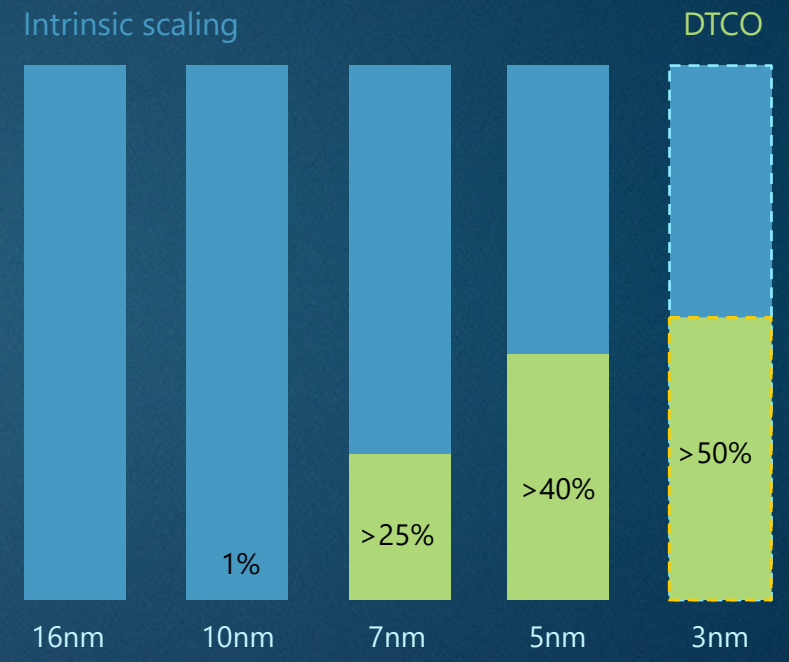
APPLIED MATERIALS®

Future of Logic Scaling

Scaling lever	Current	Inflections
Pitch scaling	 EUV EUV SADP	 + Material engineering to improve variability and reduce process steps
DTCO	 Pitch reduction	 Scaling using novel schemes

DTCO = Design Technology Co-Optimization

Pitch and DTCO scaling



Source: M. Liu/tsmc, ISSCC 2021

Increasing use of DTCO for scaling

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APPLIED MATERIALS®
make possible

PART 3

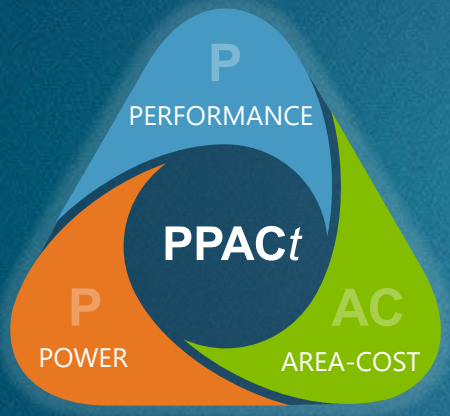
Logic Opportunities and Momentum

Raman Achutharaman, Ph.D.
Group Vice President
Semiconductor Products Group

LOGIC MASTER CLASS | June 16, 2021

Applied Materials External Use

Playbook and Growth Drivers



New architectures/ New devices	Specialty devices, mature nodes (IoT), custom ASIC
New structures/3D	Future 3D devices favoring our served markets
New materials	Low resistance metals, high-speed DRAM periphery
New ways to shrink	Materials-enabled patterning, EUV enablement
Advanced packaging	Fine-pitch interconnect for multi-chip system integration
Accelerate time-to-market	Actionable insight: e-Beam, sensors + metrology + AI/ML

’20 to ’24
Rev oppty. **+$7B**
Rev CAGR 13%
WFE CAGR 8 to 9%

IoT = Internet of Things ASIC = Application-specific Integrated Circuit eBeam = Electron Beam

Applied Materials External Use

Memory Master Class

Growing by Enabling the Capacitor Roadmap

$1B cumulative TAM opportunity

>4X annual revenue growth

Breaking tradeoffs: area, capacitance, variability

Innovative technologies + acceleration with co-optimization + acceleration with metrology

Delivering node-over-node PPAC*t* gains
↑performance, ↑yield, ↓area

DTOR / PTOR at major DRAM customers

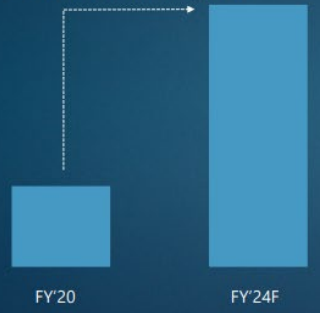
DTOR = Development Tool of Record
PTOR = Production Tool of Record

Applied Materials External Use

Leadership in PPACt Solutions for Periphery Scaling

>$2B cumulative TAM opportunity

>3X annual revenue growth



Leadership products for HKMG transistors and interconnects

Decades of experience with logic-like processing

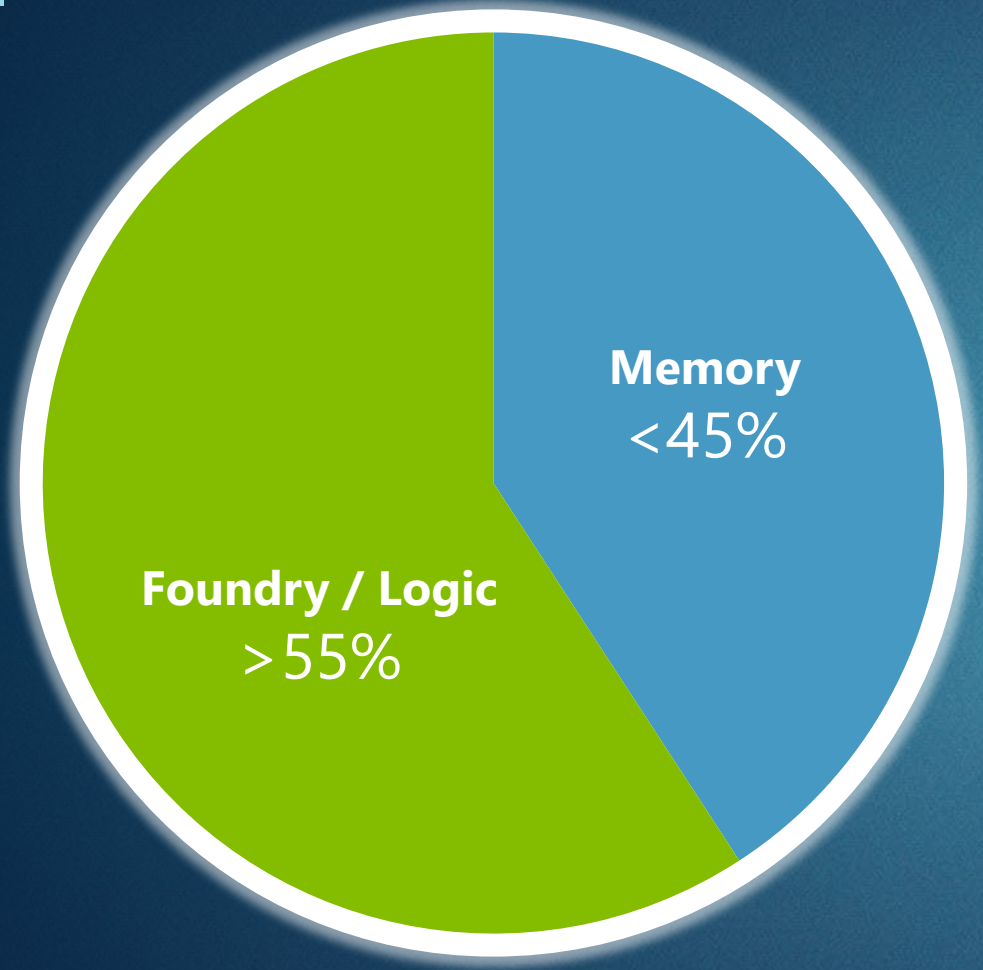
Delivering node-over-node PPAC*t* gains
↓power ,↑performance, ↑yield, ↓area

DTOR / PTOR at major DRAM customers

DTOR = Development Tool of Record
PTOR = Production Tool of Record

Applied Materials External Use

Historical WFE Mix



Long-Term Average

Foundry / Logic vs. Memory mix consistent over time

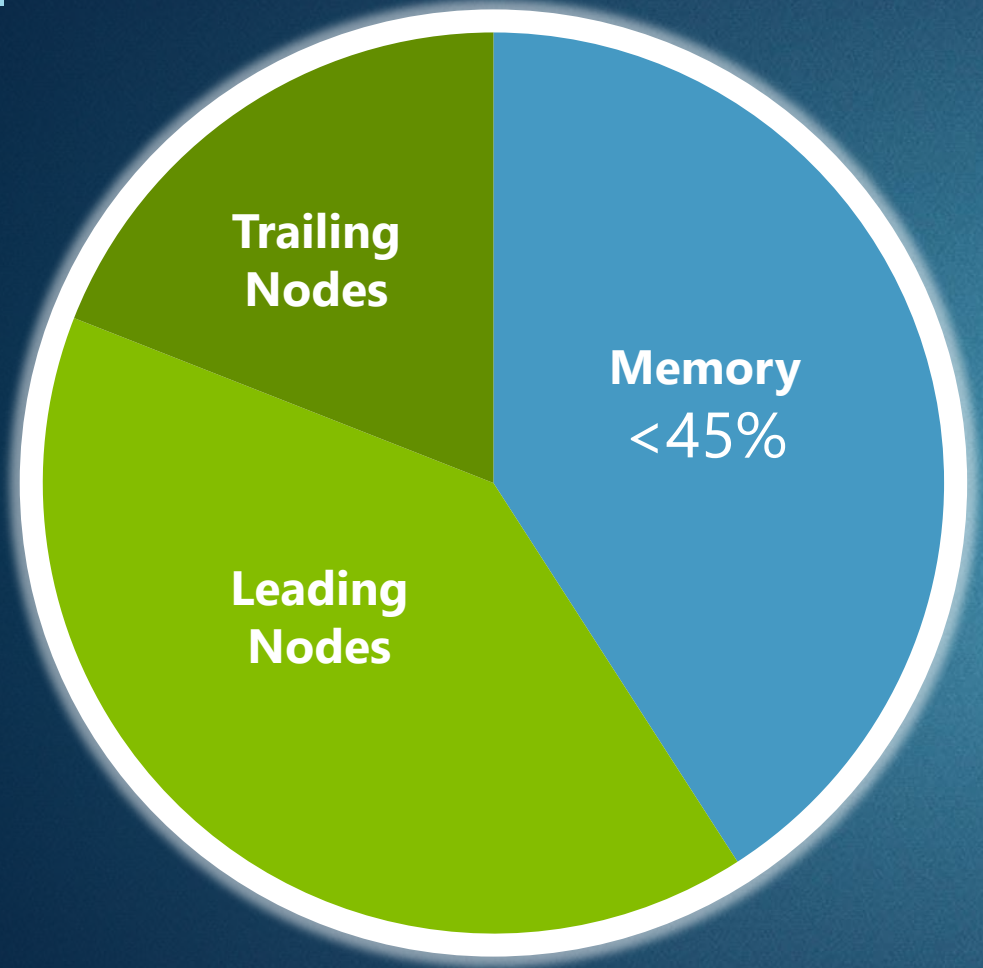
- 10-year and 20-year averages: Foundry / Logic >55%
- Foundry / Logic > Memory in 17 of past 20 years

Source: Gartner, VLSI, Applied Materials

Applied Materials External Use

APPLIED MATERIALS®

Historical WFE Mix



10-Year Average

Foundry / Logic vs. Memory mix consistent over time

- 10-year and 20-year averages: Foundry / Logic >55%
- Foundry / Logic 10-year average: Leading nodes ~2/3 Trailing nodes ~1/3

Source: Gartner, VLSI, Applied Materials

Applied Materials External Use

APPLIED MATERIALS®

ICAPS Focused on Trailing Node Foundry-Logic

Applied Materials External Use

APPLIED MATERIALS®

Packaging Grows by Enabling Higher Performance

Intel leans hard on advanced chip packaging technologies in battle for computing supremacy
SEP 16, 2020 | VENTUREBEAT

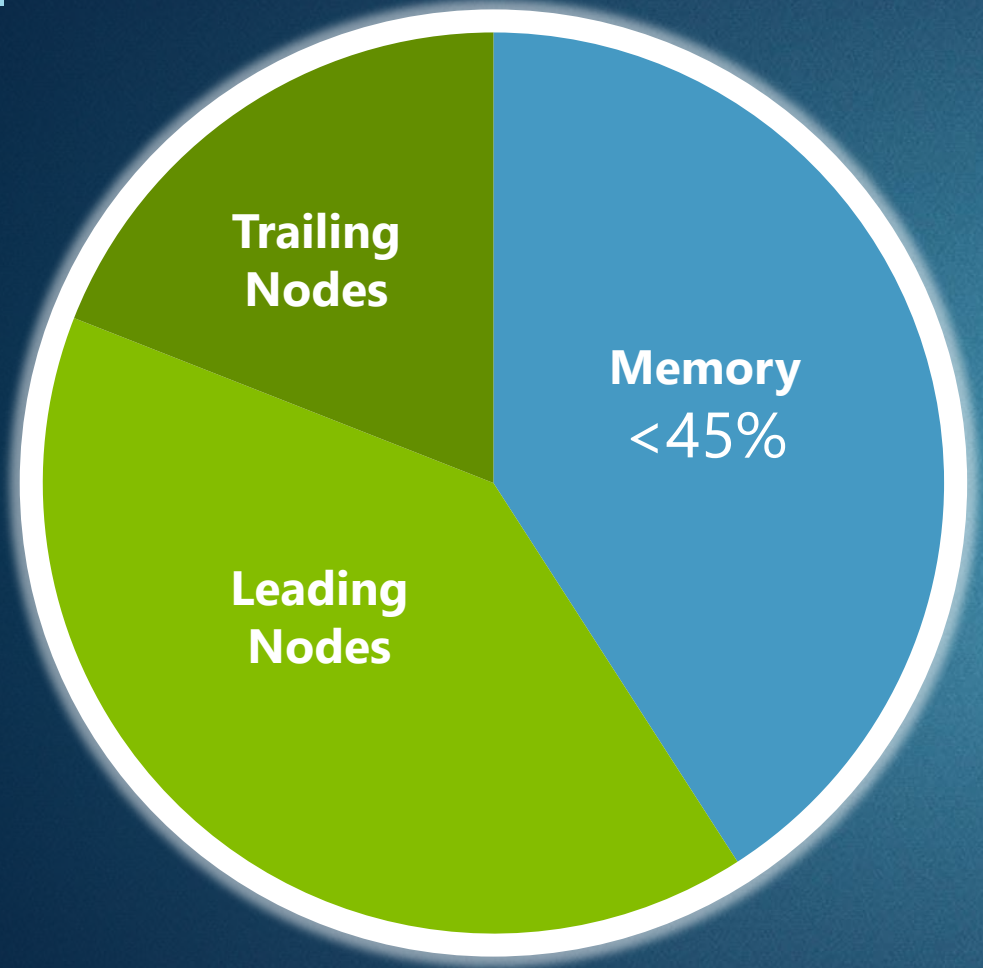
TSMC and Google look to chip packaging to boost computing power
NOV 19, 2020 | TAIWAN NEWS

AMD 3D Stacks SRAM Bumplessly
JUN 7, 2021 | WIKICHIP

Banner year for OSATs
JUN 7, 2021 | ELECTRONICSWEEKLY

Applied Materials External Use

Historical WFE Mix



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Source: Gartner, VLSI, Applied Materials

Applied Materials External Use

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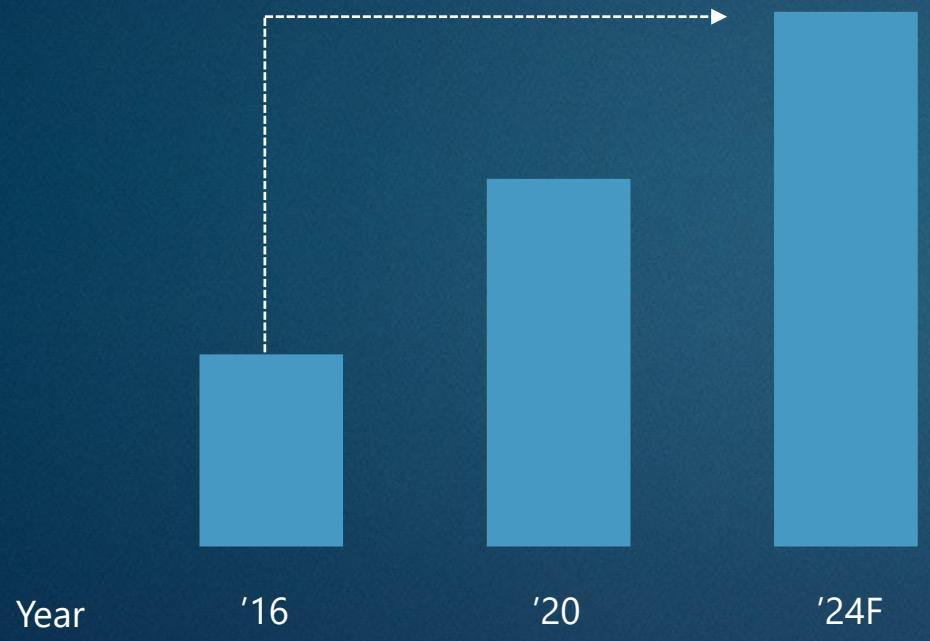
Foundry/Logic Growth Trends

>2.75x growth in spending



Logic / Foundry WFE expansion with digital transformation of the global economy

Increasing process complexity

Leading edge drives 2/3 of Foundry/Logic WFE

Applied Materials External Use

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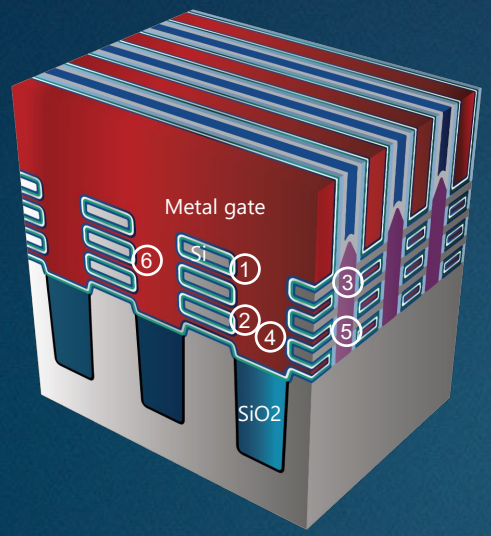
Enabling the Transistor Roadmap: Gate-All-Around



FinFET → GAA (value gains)

↓ leakage/power (geometry)

↑ drive current/speed (stacking)

↑ density (narrower sheet width)

↓ variability (epi defined vs. litho/etch)

↓ 25-30% power; ↑ 10-15% performance#

KEY NEW MODULE STEPS	REQUIREMENTS
① Super lattice epitaxy	Sharp interfaces, thickness control
② Selective removal	Etch selectivity, no nanosheet collapse
③ S/D stressors (etch, epitaxy)	Controlled recess & growth
④ Metal gate between nanosheets	New materials + void-free gapfill
⑤ Inner spacer (sel. removal, dep)	Controlled lateral recess, gapfill
⑥ Super lattice metrology	Buried defect detection, measurement

New process steps + increased complexity of existing steps

~ $1B TAM incremental opportunity*

#SAFE - Samsung Advanced Foundry Ecosystem, Oct 2020
* 100K WSPM
S/D = Source / Drain

Applied Materials External Use

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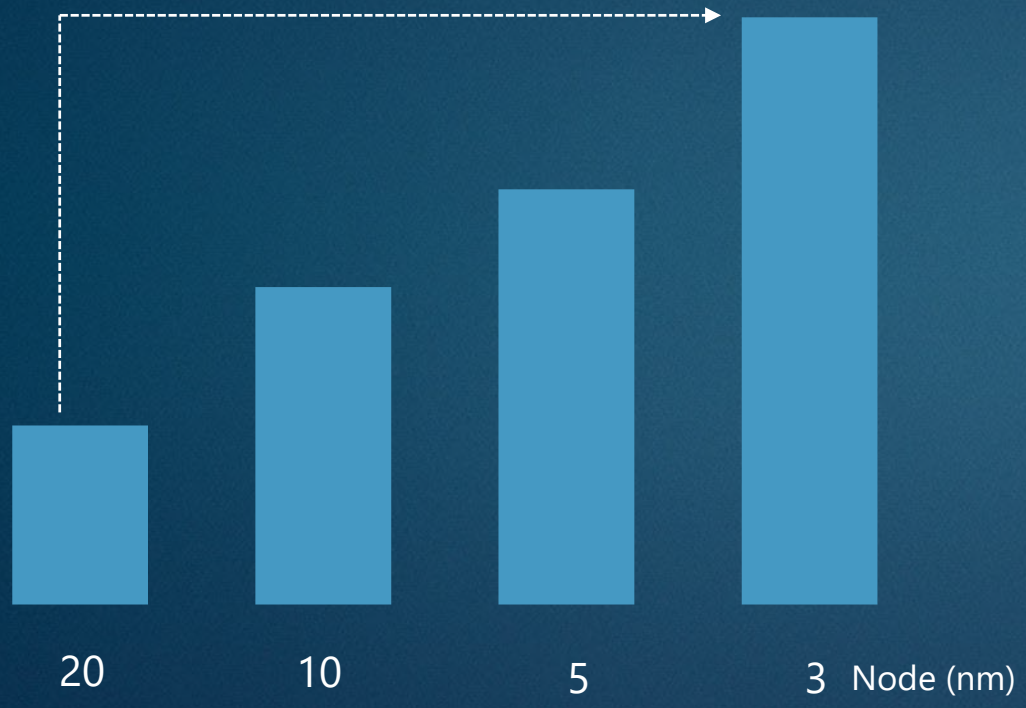
Enabling the Interconnect Roadmap

>2X process step growth

>3X TAM growth



>30 years of PVD market leadership
>25,000 Endura® installed base chambers

Breakthrough technologies + new materials + unique combinations + interface engineering

Delivering node-over-node PPACt™ gains
↓ R, ↓ power, ↑yield, ↑reliability, ↓ area

PVD = Physical Vapor Deposition

Applied Materials External Use

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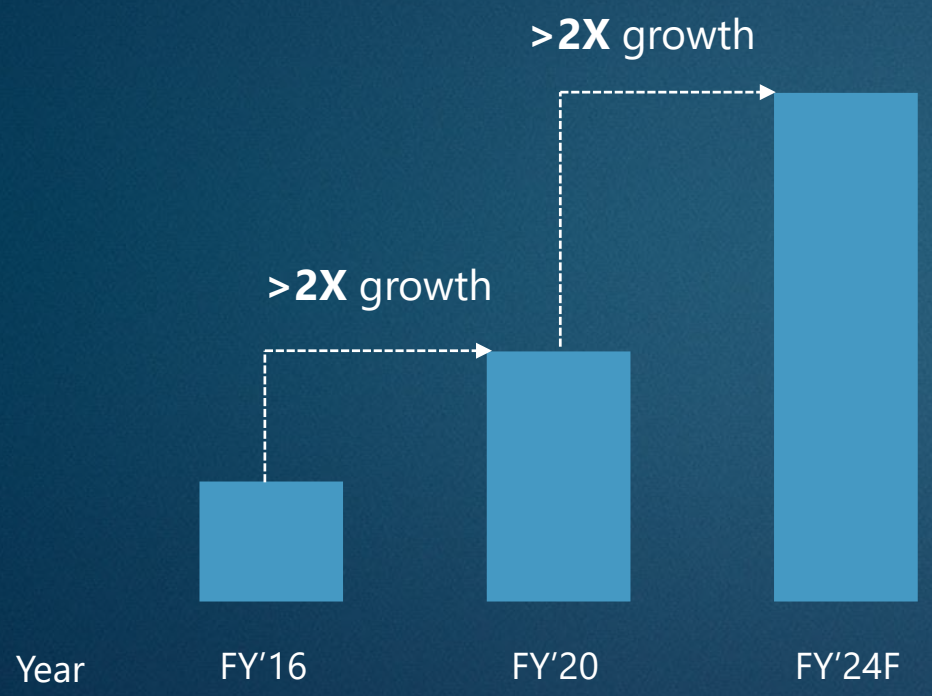
Patterning Growth Driven by New Products

>$3.5B cumulative revenue next 4 years



Successful Sym3® family of etch products

New materials for hard mask and patterning

Innovative technologies + acceleration with co-optimization + acceleration with metrology

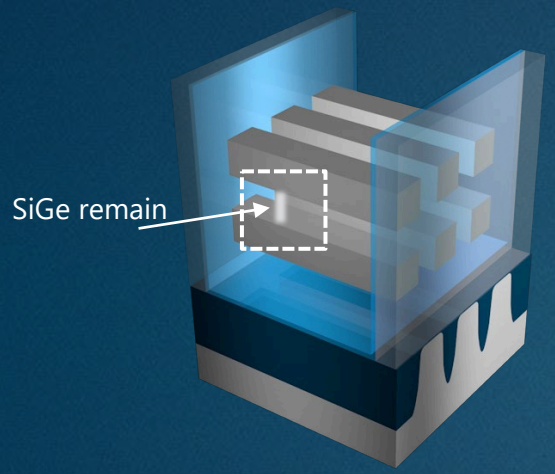
Materials enabled scaling (DTCO) complements traditional pitch scaling

Applied Materials External Use

Applied's eBeam Inspection and Metrology Leadership

Unique challenges with 3D structures

eBeam inspection

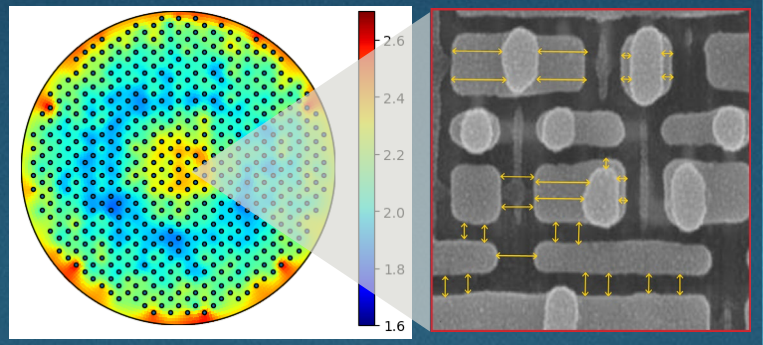


Gate-All-Around

Finding buried defects in 3D structures 5X faster

Full wafer statistics needed

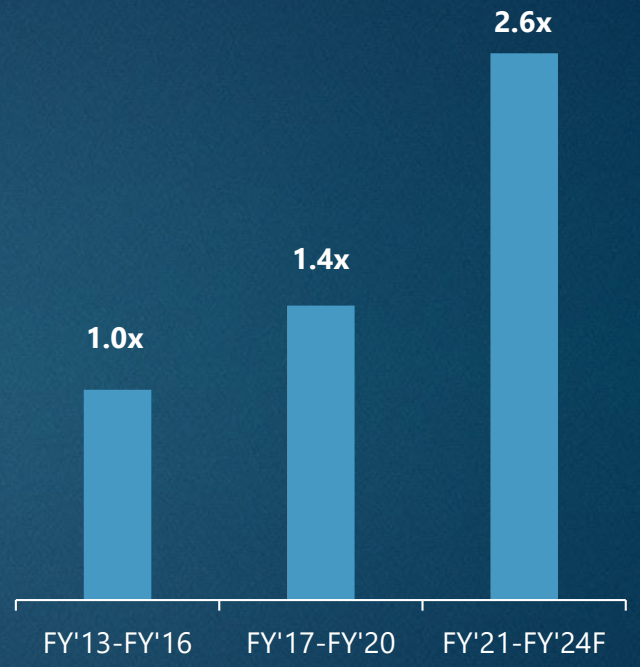
eBeam metrology



In-device CD and overlay

Enabling millions of data points to provide full-wafer actionable data

Driving revenue growth



Imaging + Process Control

Actionable insights. PPACt™ acceleration.

Applied Materials External Use

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APPLIED
MATERIALS®
make possible