New Ways to Shrink: Advanced Patterning Products Launch

Applied Materials News from the
2023 SPIE Advanced Lithography + Patterning Conference

February 28, 2023

Forward-Looking Statements and Other Information

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our market share positions, our development of new products and technologies, our products' expected cost savings and environmental benefits, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; our ability to accurately forecast cost savings and environmental benefits from using our products; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

WELCOME

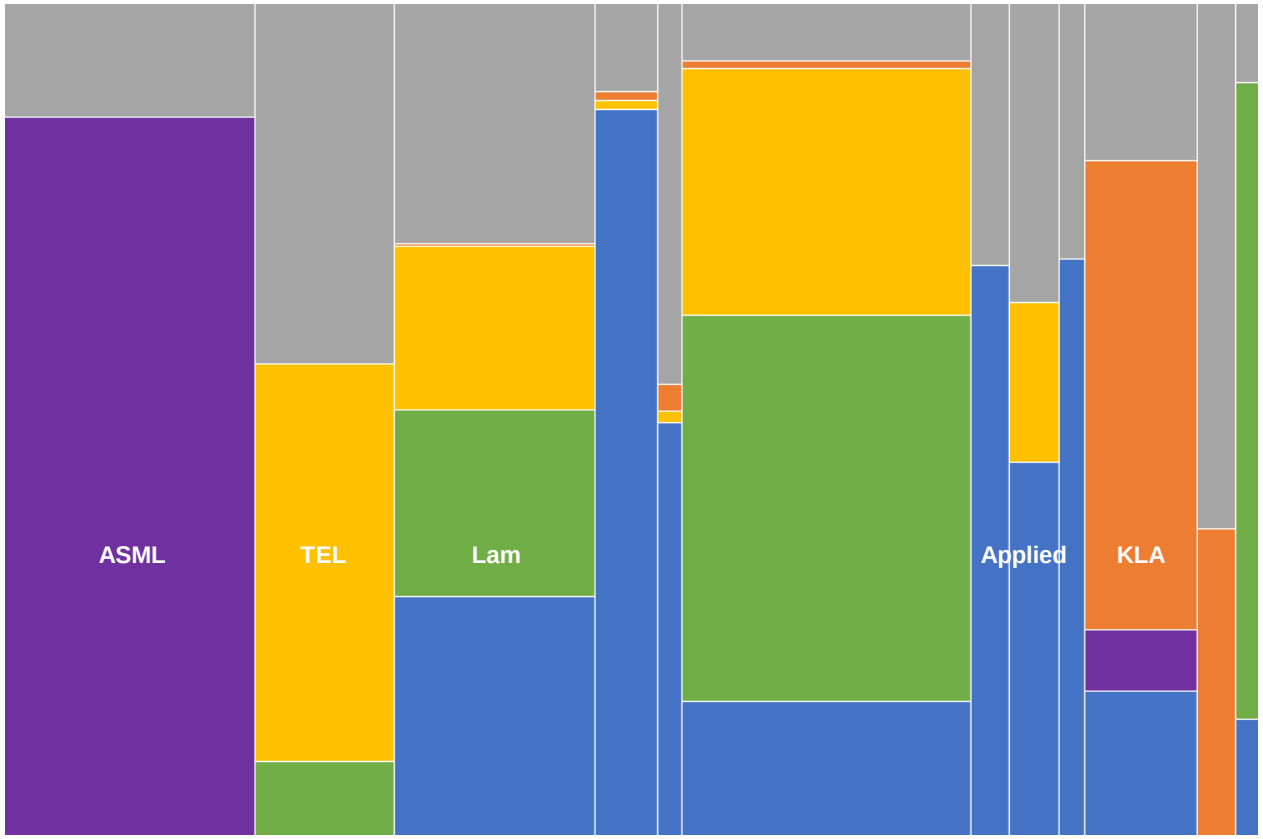
Michael Sullivan

Corporate Vice President

Head of Investor Relations

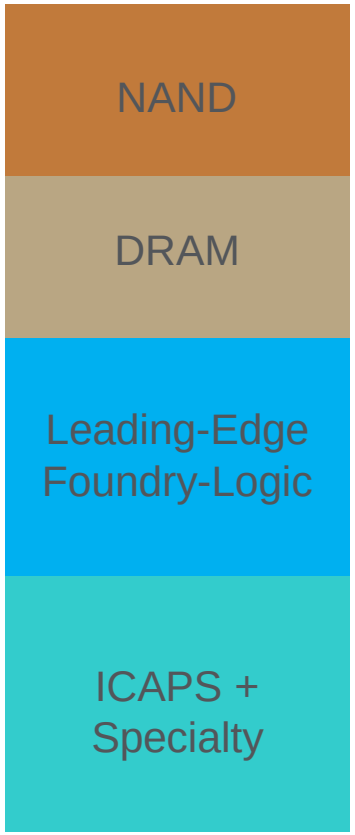
Semiconductor Wafer Fab Equipment Market Segmentation

By Equipment Type



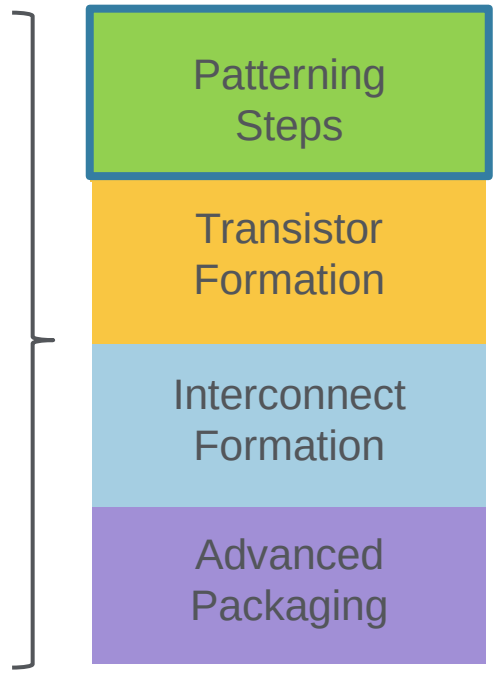
Source: TechInsights, 2021

By Device Type



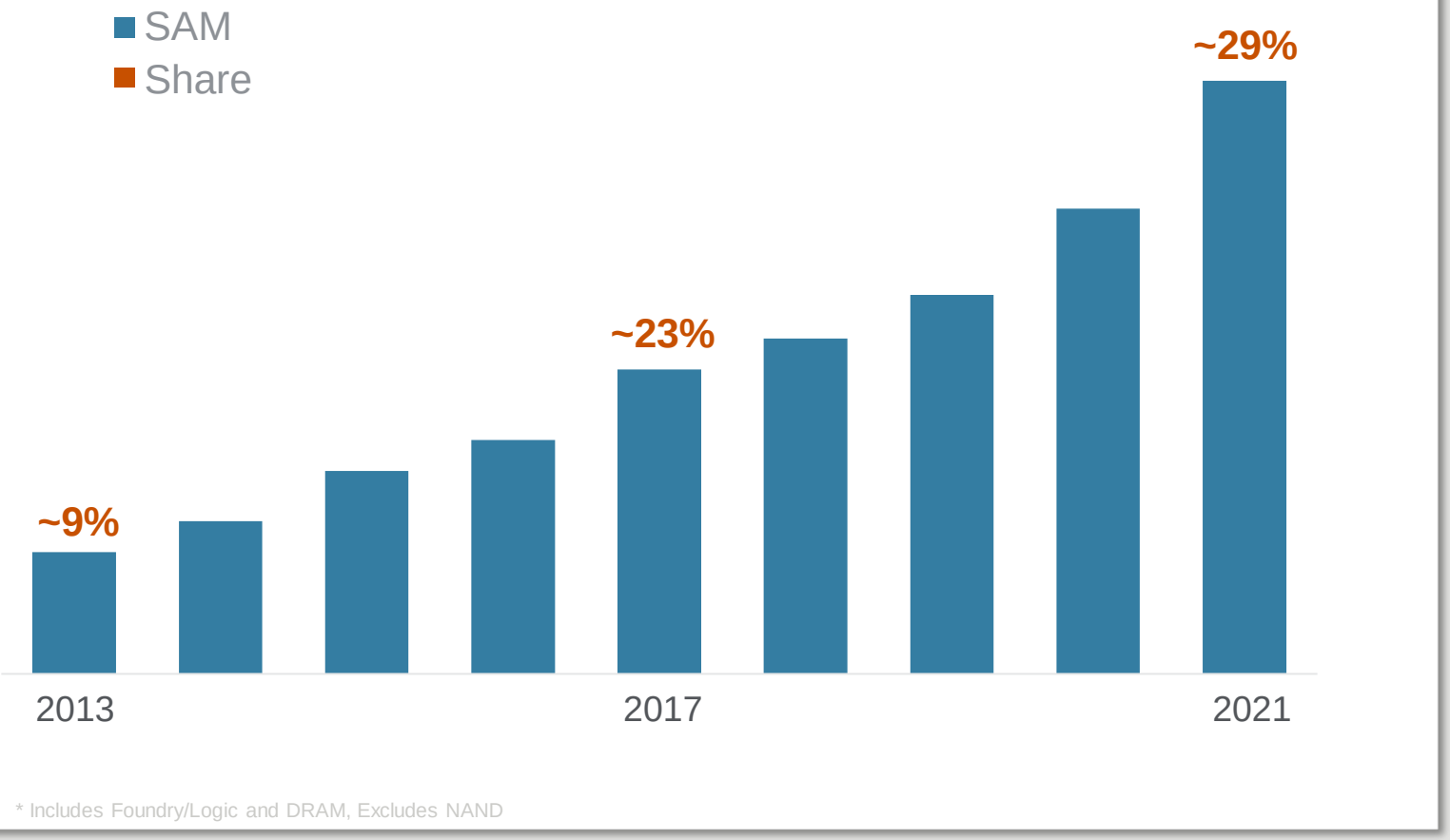
Source: Applied Materials 2021

By Application



Market sizes not to scale

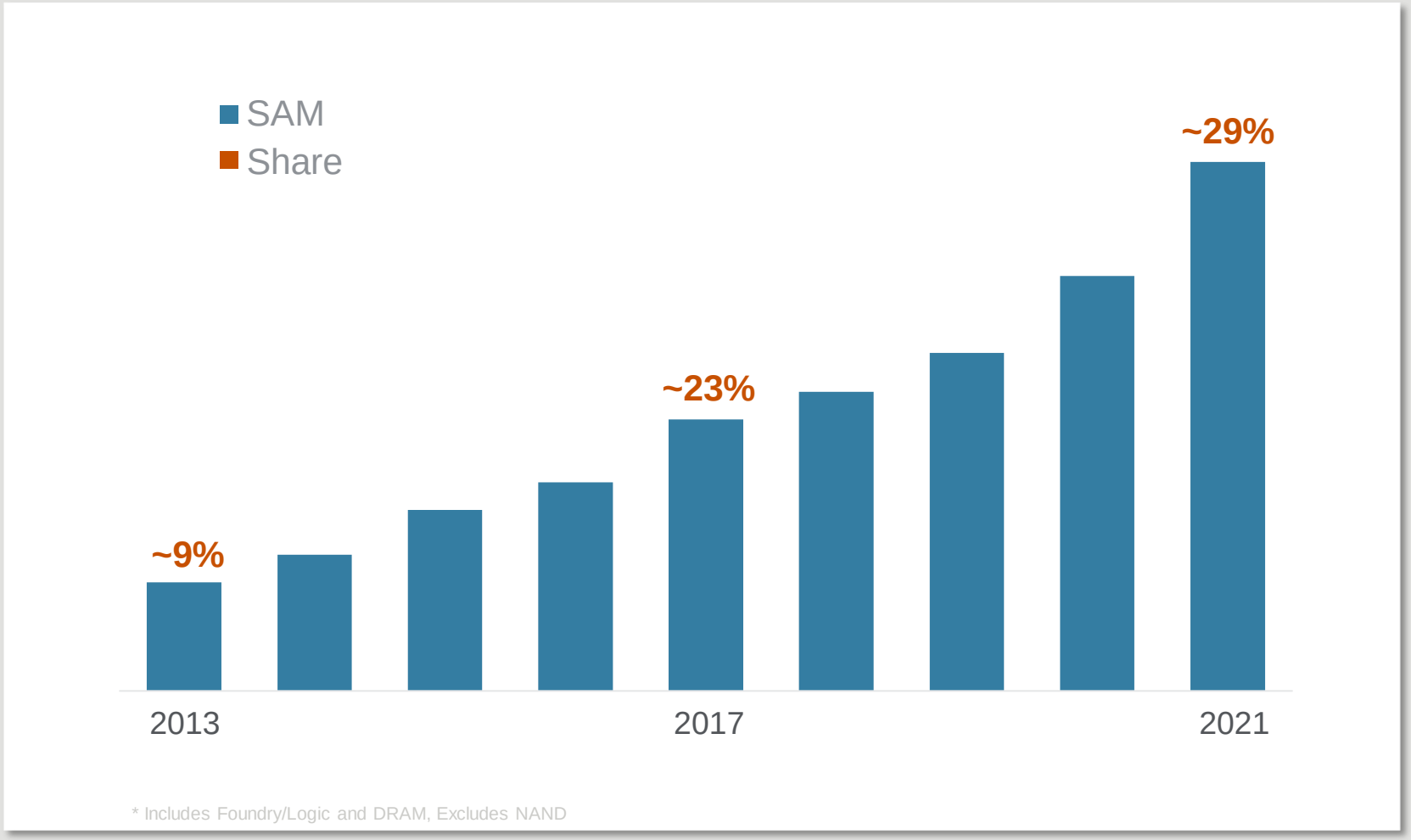
Applied Materials Patterning Served Markets and Share



Industry's Broadest Portfolio
ALD
CMP
CVD
Etch
Metrology
NEW
Selective Materials Removal
Thermal

Applied's patterning SAM has grown at 1.4X the rate of WFE

Applied Materials Patterning Served Markets and Share



Industry's Broadest Portfolio
ALD
CMP
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Metrology
NEW: Pattern Shaping
Selective Materials Removal
Thermal

Applied's patterning SAM has grown at 1.4X the rate of WFE

AGENDA

Steven Sherman
New Pattern-Shaping Technology Reduces EUV Steps

Keith Wells
New CD-SEM Technology Paves the Way to High-NA EUV

Q&A

Introducing Pattern Shaping

Steven Sherman

Managing Director, GM, Advanced Products Group

Semiconductor Products Group

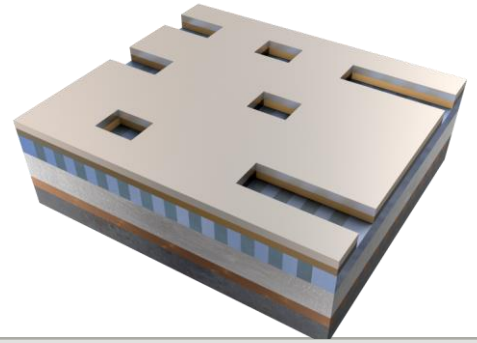
Creating Patterns with EUV Lithography

LINES / GRATING

Create lines and spaces

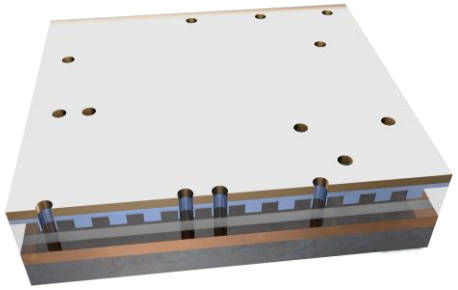
CUTS

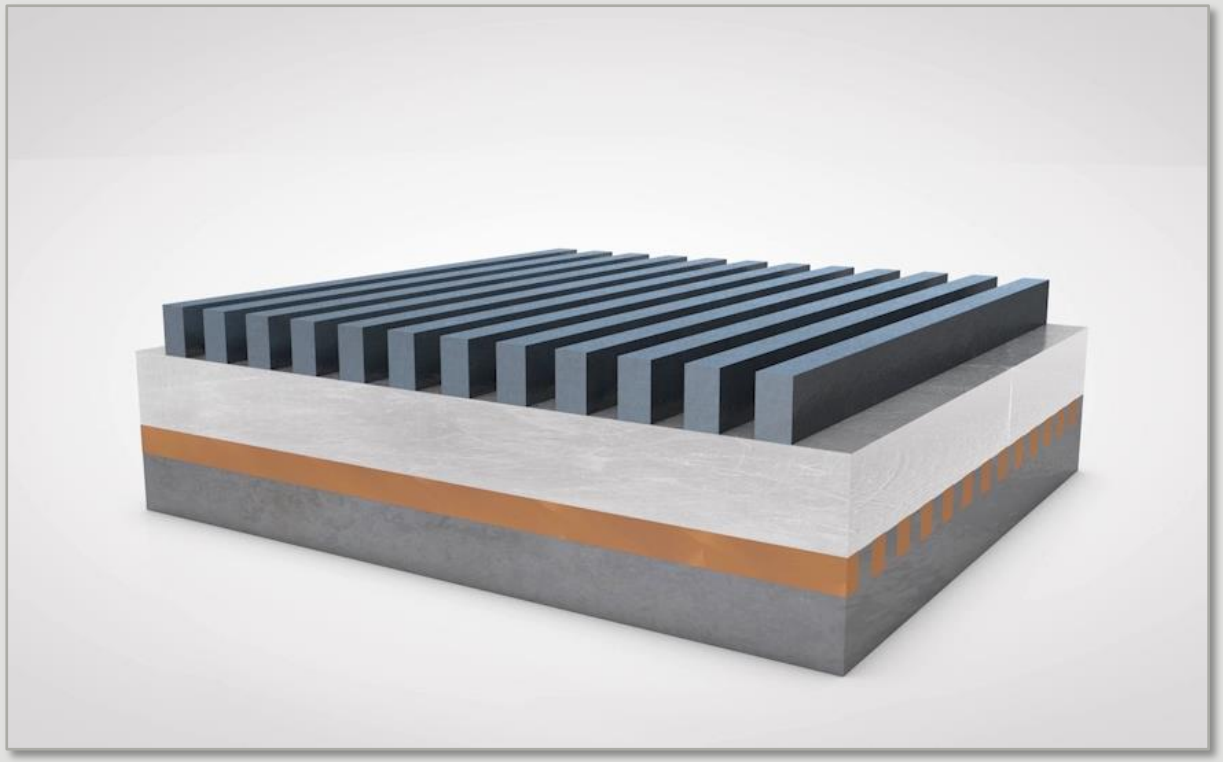
Segment lines



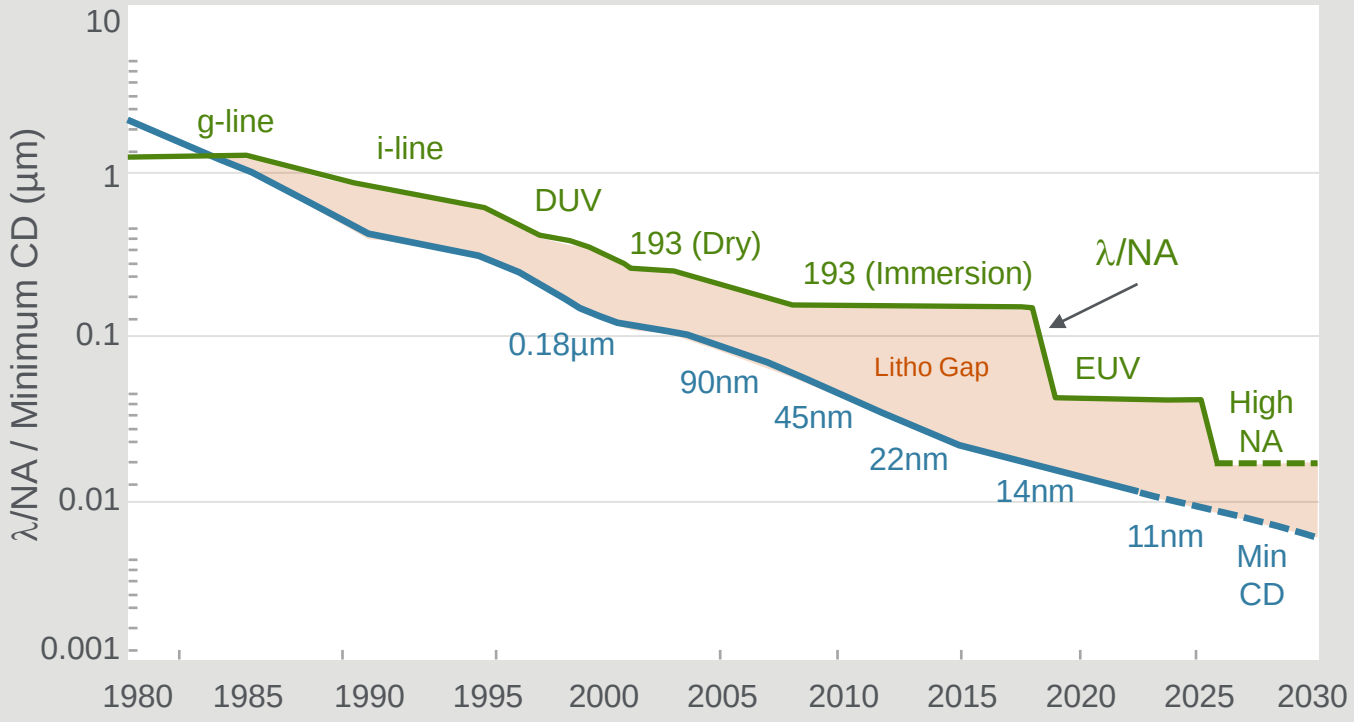
VIAS

Connect layers

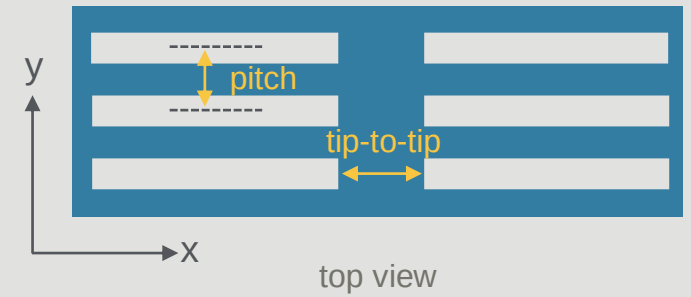




Pitch Scaling Roadmap

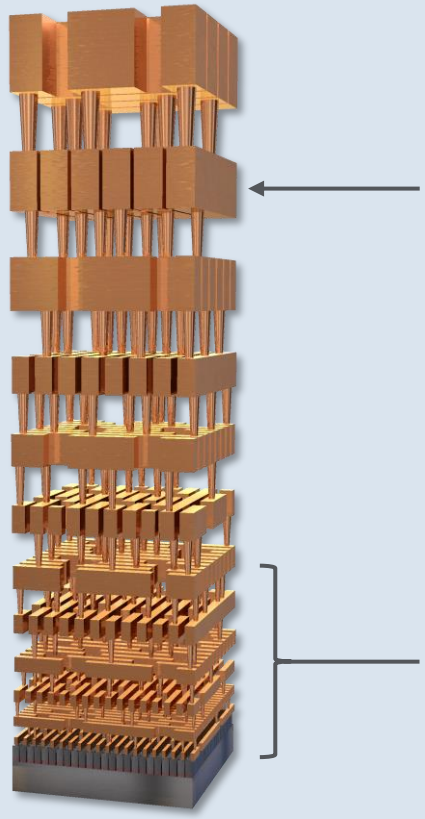


Patterning scheme	Minimum tip-to-tip at line/space pitch of ~32nm
EUV Single Patterning	~25-30nm
EUV Double Patterning	~15-20nm



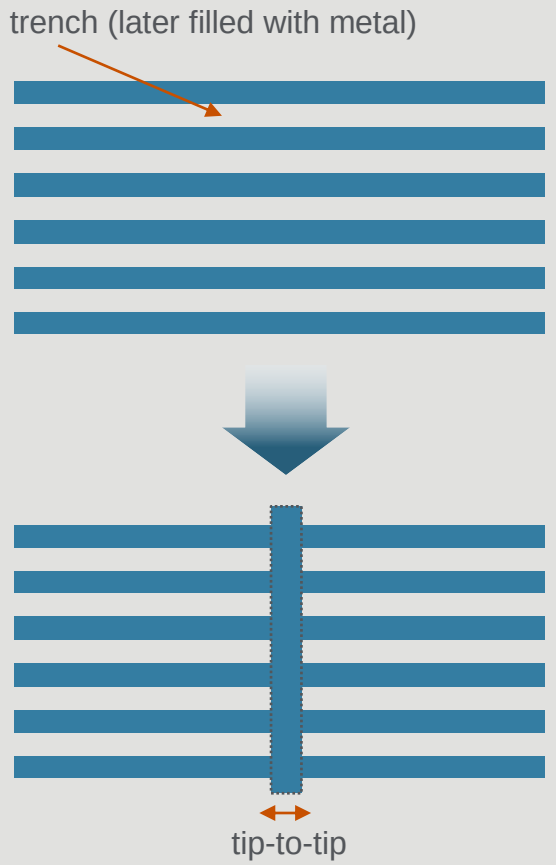
top view

EUV Double Patterning Example: Dense Interconnect Lines



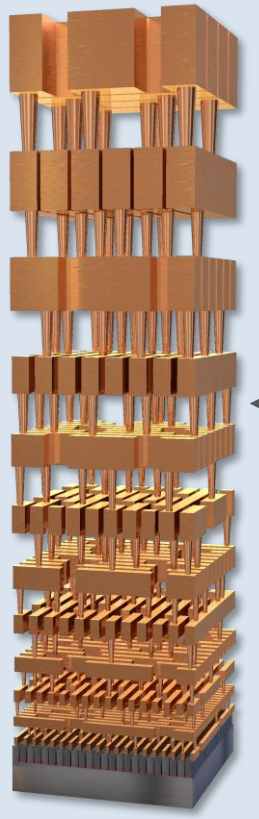
metal lines route signals and power within each layer of a chip

multi-patterning used in the smallest, most critical layers



Tighter tip-to-tip spacing enables higher device density, which optimizes die area

EUV Double Patterning Example: Dense Vias

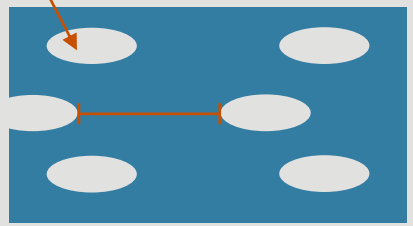


vias: connect metal layers

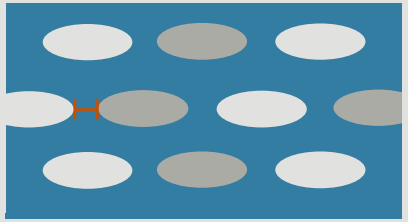
multi-patterning used in the smallest, most critical layers

via (later filled with metal)

EUV litho-etch 1
vias patterned with relaxed tip-to-tip spacing



EUV litho-etch 2
vias doubled with tight tip-to-tip spacing

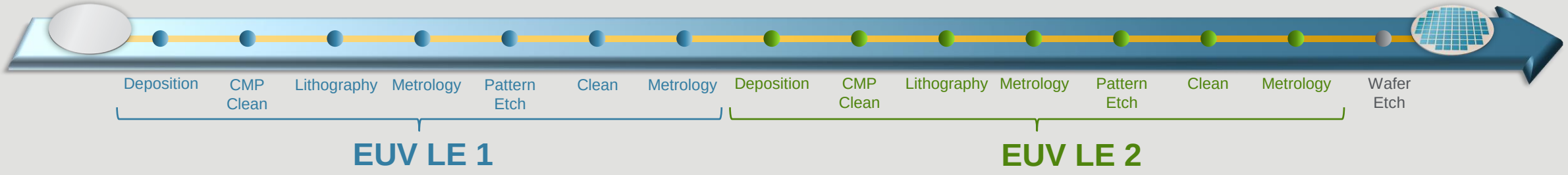


top view

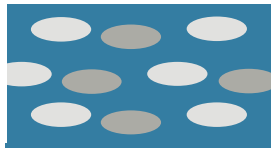
Elliptical vias provide larger electrical connection areas which optimize power, performance and yield
Tighter tip-to-tip spacing increases via density which optimizes die area and cost

EUV Double Patterning Process Flow

Simplified Litho-Etch Litho-Etch (LELE) Process Flow



Alignment errors



Can cause:

- litho rework cost
- chip performance/ power issues
- yield loss

Per-EUV LE energy and materials

~25kWh per wafer

~0.5kg CO_2 eq. per wafer

~15L per wafer

Per-EUV LE cost

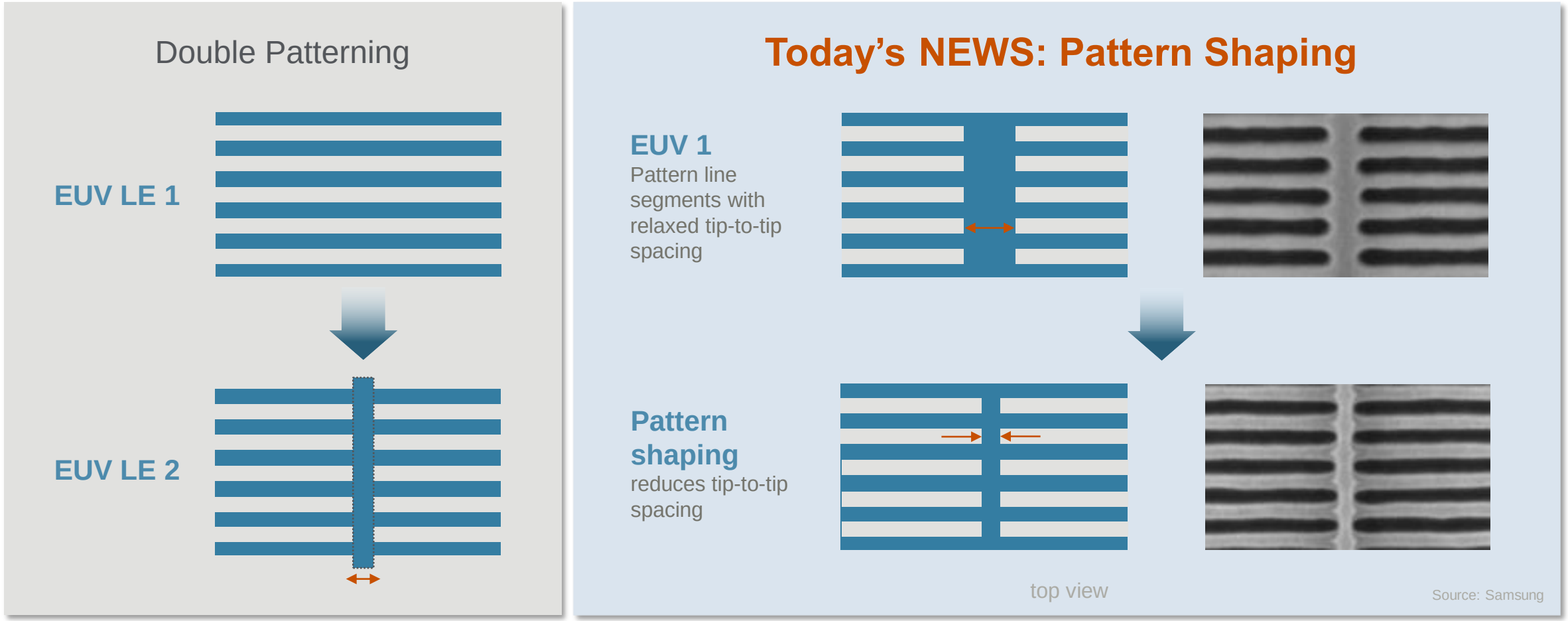
~$350M capital cost per 100K WSPM fab

~$70 per wafer

Source: Applied Materials and imec.netzero v0.2.89 IC chip footprint calculator

Double patterning steps add cycle time, process complexity, energy, materials usage and cost

Pattern Shaping Alternative to EUV Double Patterning: Interconnect Lines

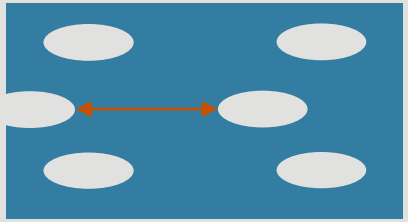


PPACt benefit: delivers the density of EUV double patterning with only one EUV step, simplifying the patterning process flow and optimizing chip area and cost

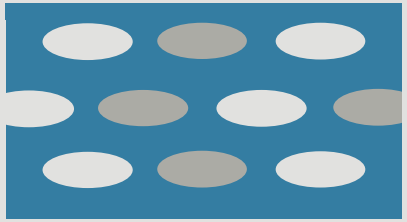
Pattern-Shaping Alternative to EUV Double Patterning: Vias

Double Patterning

EUV LE 1

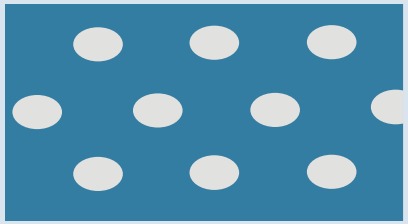


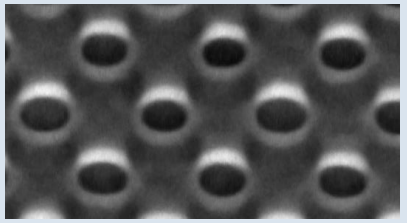
EUV LE 2



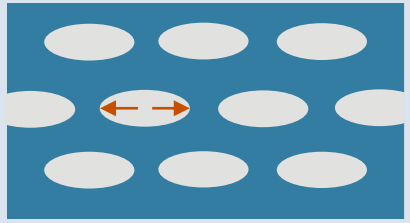
Today's NEWS: Pattern Shaping

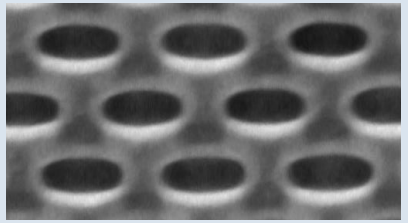
EUV 1
Pattern round vias at relaxed EUV spacing





Pattern shaping
creates elliptical vias with tight spacing





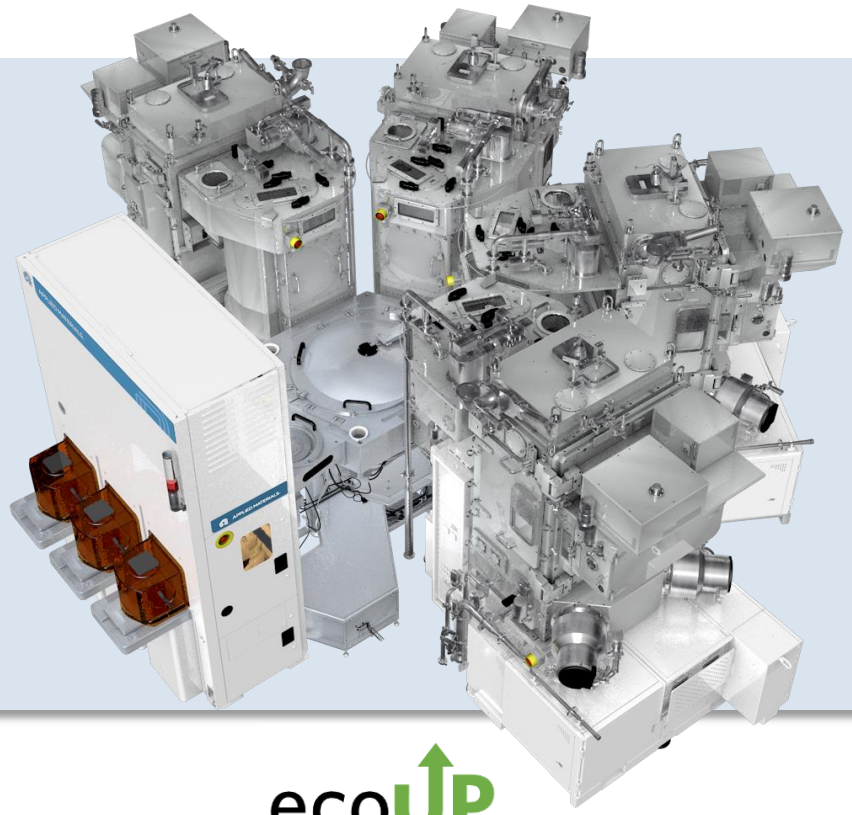
top view

Source: Applied Materials

PPACt benefit: delivers high-density elliptical vias with only one EUV step, simplifying the patterning process flow – and optimizing chip power, performance, area and cost

Introducing Centura® Sculpta® Patterning System

A breakthrough innovation for the patterning engineer's toolkit



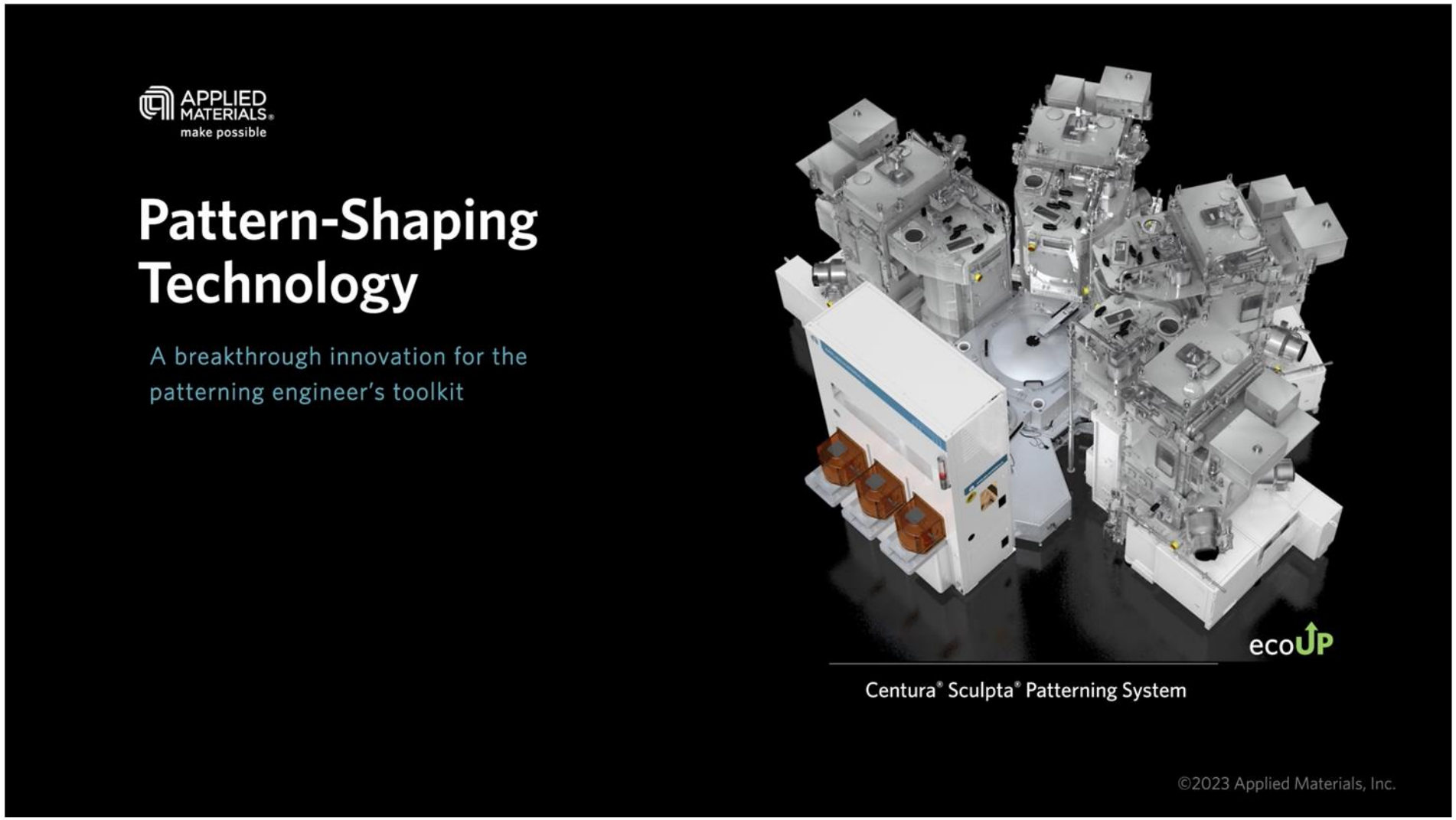
- ✓ Enhances EUV patterns to optimize chip area and cost without EUV double patterning
- ✓ Reduces patterning complexity to increase yield
- ✓ Reduces the environmental impact of advanced chipmaking by saving energy, materials and water
- ✓ Reduces capital and operating costs
- ✓ Extendable to high-NA EUV patterning

ecoUP

In development for over 6 years with leading customers

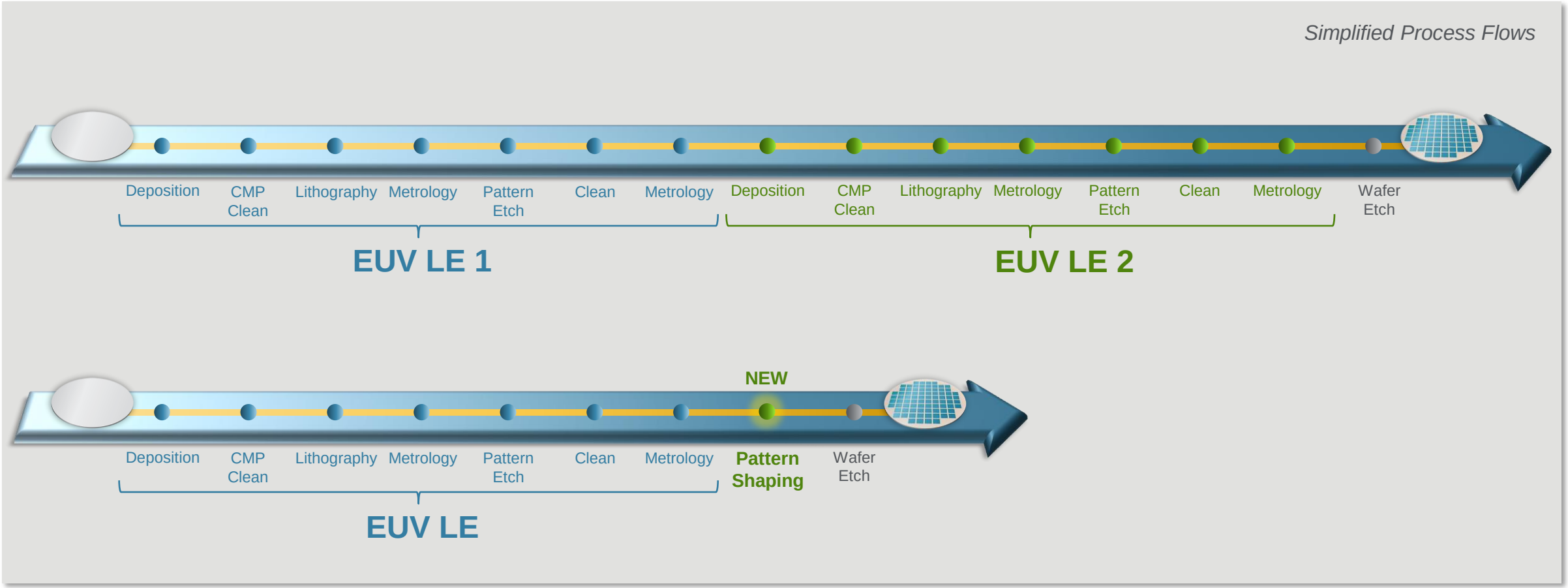
Production tool of record for multiple layers in leading-edge logic

Animation: How Pattern Shaping Works



YouTube link: https://youtu.be/GSuTyOMq1Bg

Pattern-Shaping Process Flow

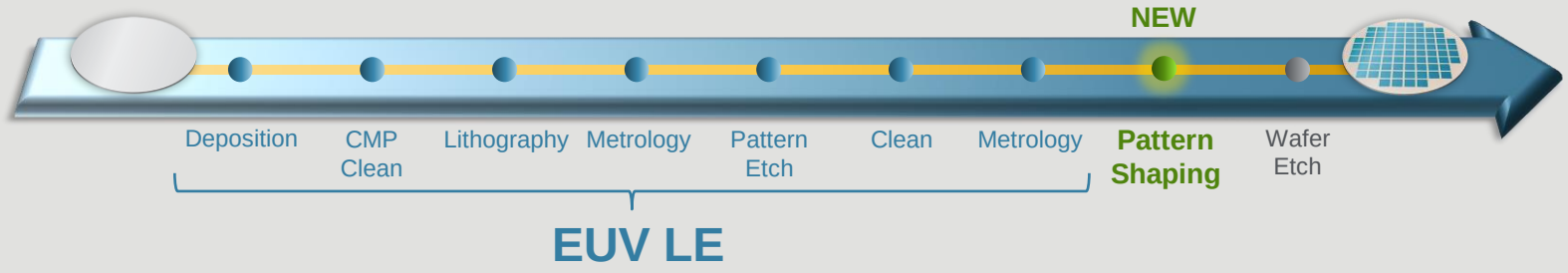


Source: Applied Materials

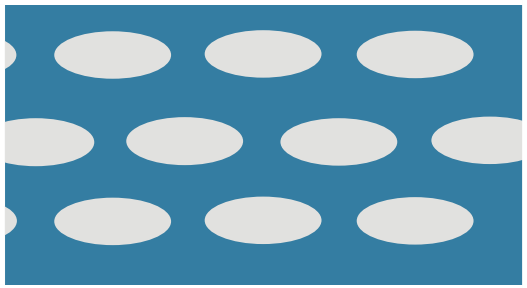
Pattern shaping replaces one EUV LE process loop,
saving design and process complexity, cycle time, energy, materials usage and cost

Benefits of Pattern Shaping

Simplified Litho-Etch (LE) Plus Pattern-Shaping Process Flow



No alignment errors



Per-layer energy + materials savings

>15kWh per wafer

>0.35kg CO_2 eq. per wafer

~15L per wafer

Per-layer cost savings

~$250M capital cost per 100K WSPM fab

~$50 per wafer

Source: Applied Materials and imec.netzero v0.2.89 IC chip footprint calculator

Reduces design and process complexity, cycle time, energy, materials usage and cost

Breakthrough Innovation for the Patterning Engineer's Toolkit

Press Release

Applied Materials' Innovative Pattern-Shaping Technology Reduces the Cost, Complexity and Environmental Impact of Advanced Chip Manufacturing

- *The new Centura® Sculpta® patterning system provides a simpler, faster and more cost-effective alternative to EUV double patterning*

SANTA CLARA, Calif., Feb. 28, 2023 – Applied Materials, Inc. today unveiled a breakthrough in patterning technology that allows chipmakers to create high-performance transistors and interconnect wiring with fewer EUV lithography steps, thereby lowering the cost, complexity and environmental impact of advanced chipmaking.

> *"As Moore's Law drives us to ever-greater compute performance and density, pattern shaping is proving to be an important new technology that can help reduce manufacturing cost and process complexity and conserve energy and resources. Having collaborated closely with Applied Materials in the optimization of Sculpta around our process architecture,* ***Intel will be deploying pattern-shaping capabilities to help us deliver reduced design and manufacturing costs, process cycle times and environmental impact.***"
>
> - Ryan Russell, Corporate VP for Logic Technology Development at Intel

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"*Three critical issues must be considered when pushing the limits of patterning: tip-to-tip spacing, pattern bridge defects and line edge roughness.* ***As an early development partner on the innovative pattern-shaping technology, I believe Applied's Sculpta system is a fascinating breakthrough that addresses these patterning challenges and reduces manufacturing costs for chipmakers worldwide.***"

- Jong-Chul Park, Master of Foundry Etch Technology Team at Samsung Electronics

Breakthrough Innovation for the Patterning Engineer's Toolkit

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"*Applied Materials' new Sculpta system is **a revolution in patterning that brings an entirely new capability to chipmakers**. As the industry keeps pushing the limits of chip scaling, we need breakthroughs like Applied's pattern-shaping technology that can improve chip power, performance, area and cost while also reducing design cost, and energy and materials consumption. Sculpta is **the most innovative new process step in wafer fabrication since the introduction of CMP**.*"

- Dan Hutcheson, Vice Chair, TechInsights

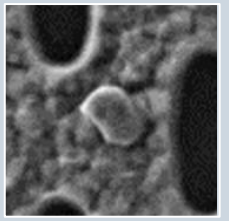
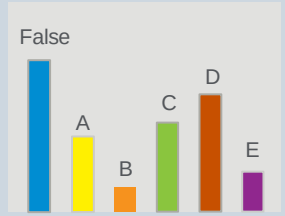
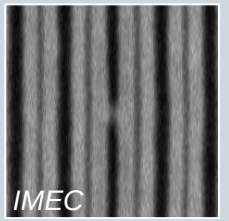
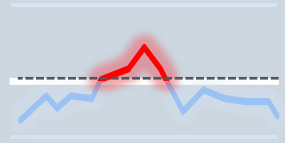
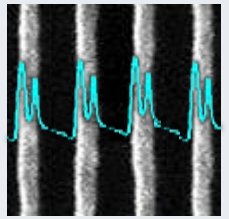
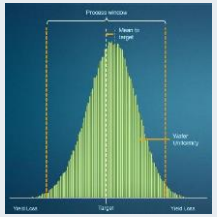
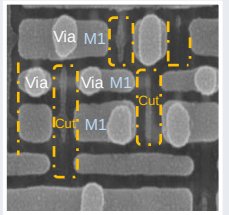
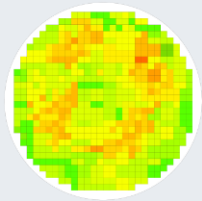
New CD-SEM Technology Paves the Way to High-NA EUV

Keith Wells

Group Vice President and General Manager

Imaging and Process Control Group

eBeam Tools: “The Eyes of the Fab”

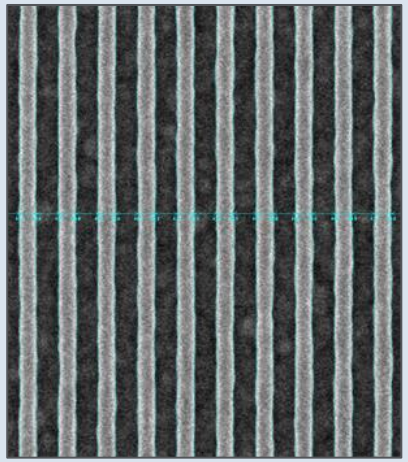
Segment	Applications	Purpose	Image	Actionable Insight
Defect Control	Defect Review **SEMVision®**	**SEE** to distinguish critical defects from noise, enable root cause analysis		
	Defect Inspection **PrimeVision®**	**DETECT** small, buried and electrical defects		
Patterning Control	CD Metrology **VeritySEM®**	**CALIBRATE** Lithography and etch processes to maximize yield		
	CDU and OVL Metrology **PROVision®**	**MEASURE** millions of locations across the wafer to characterize overlay and edge placement errors (EPE), assess CD uniformity and identify process signatures		

*CDU: critical dimension uniformity

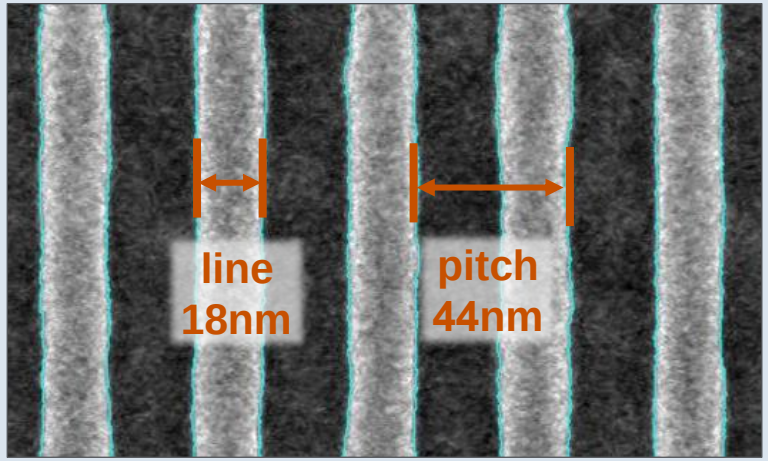
CD-SEM: “The Ruler of the Fab”

critical dimension scanning electron microscope (CD-SEM)

High-NA EUV pattern



critical dimensions (CD)

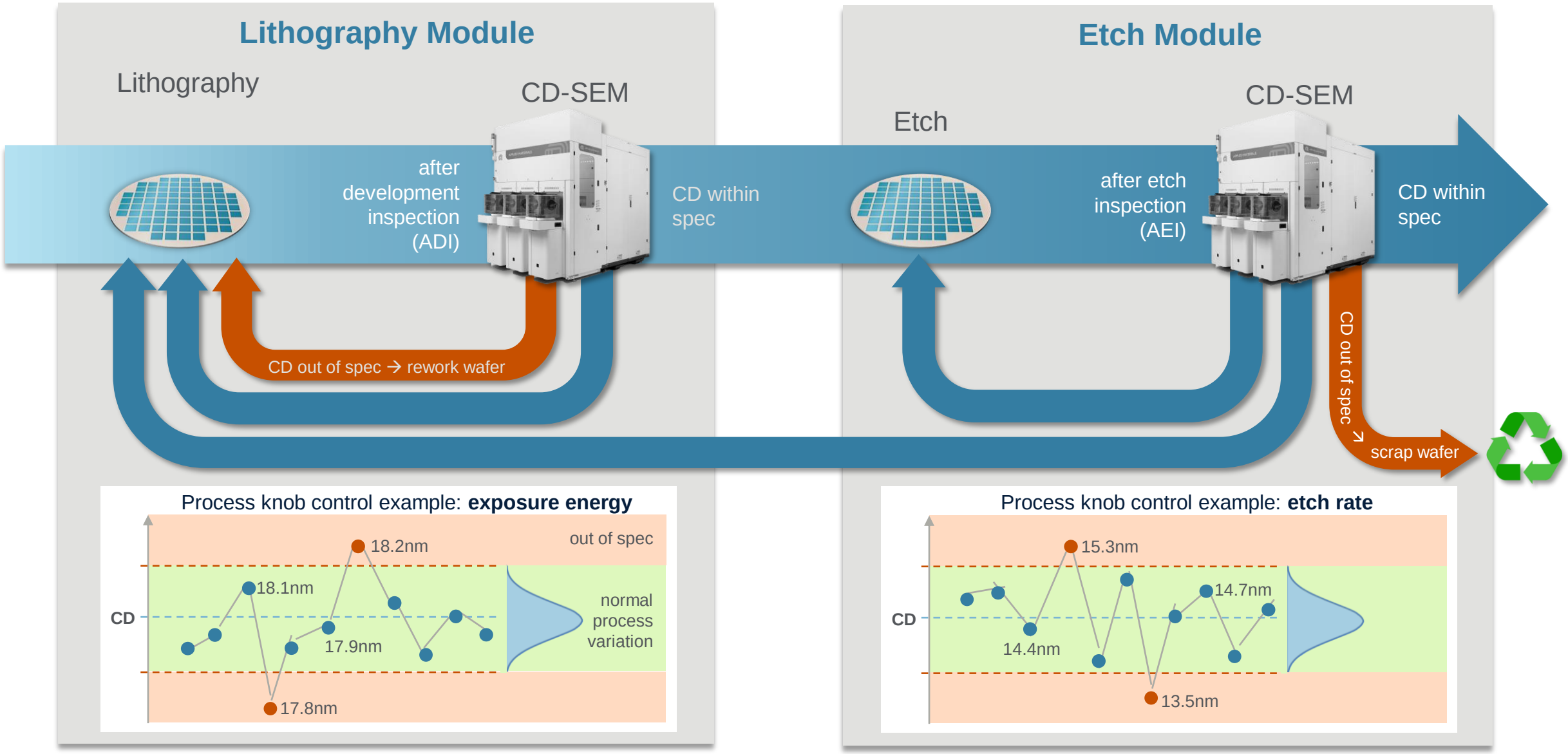


top view

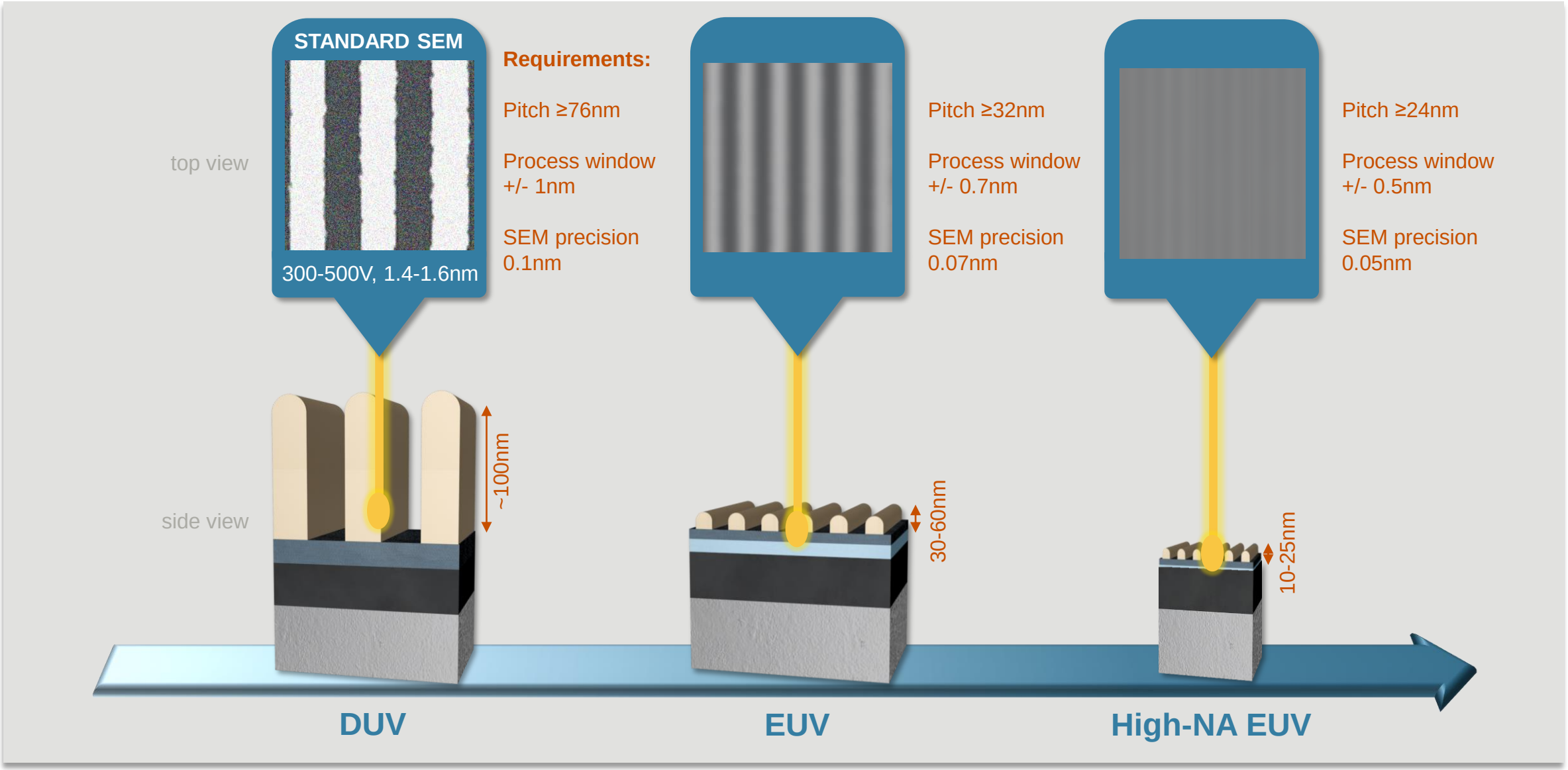
Source: Applied Materials

CD-SEM produces precise, sub-nanometer measurements to continuously calibrate lithography process performance

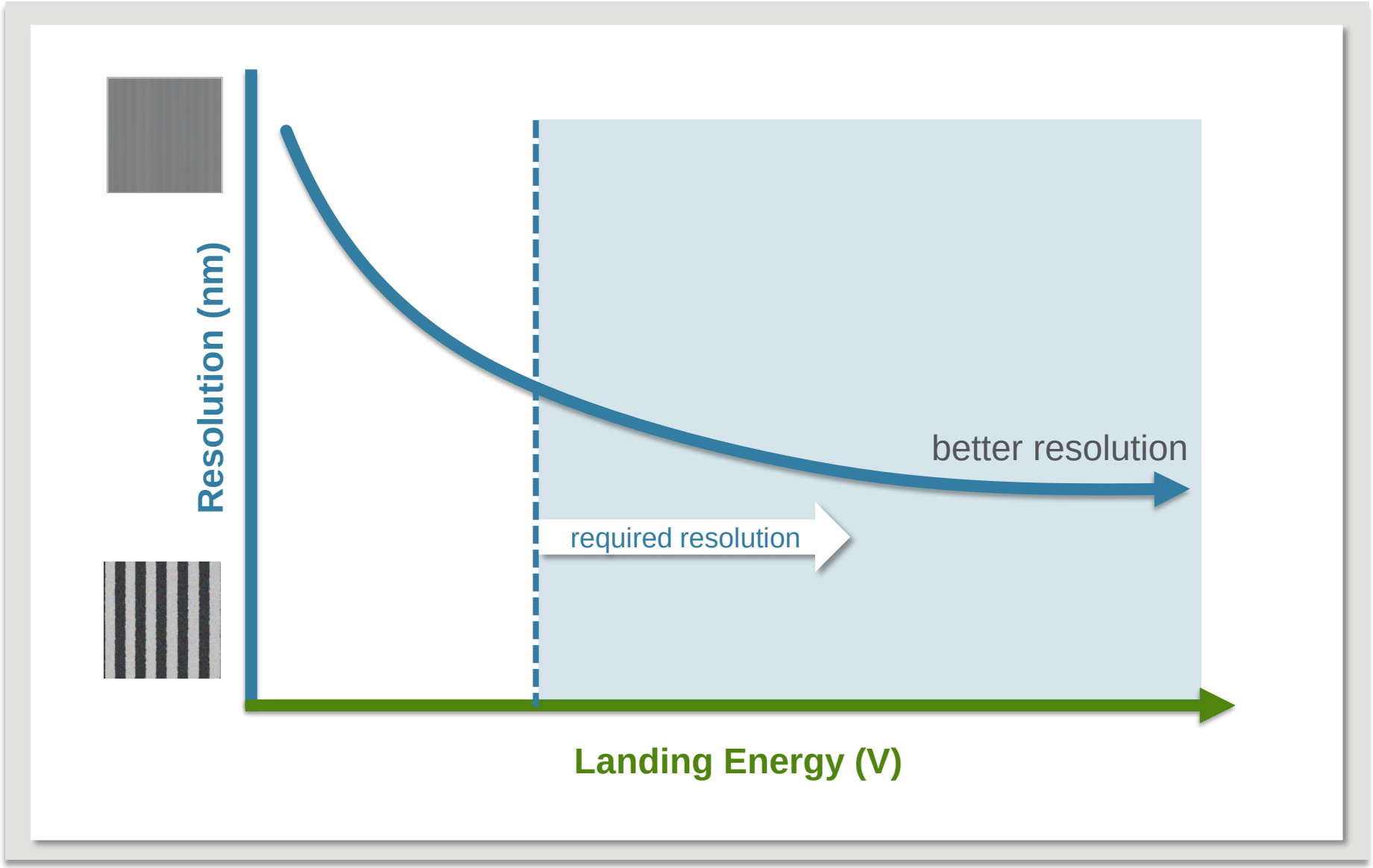
CD-SEM: Helping Control Lithography and Etch Patterning Flows



EUV Patterning Requires CD-SEM eBeam Innovations

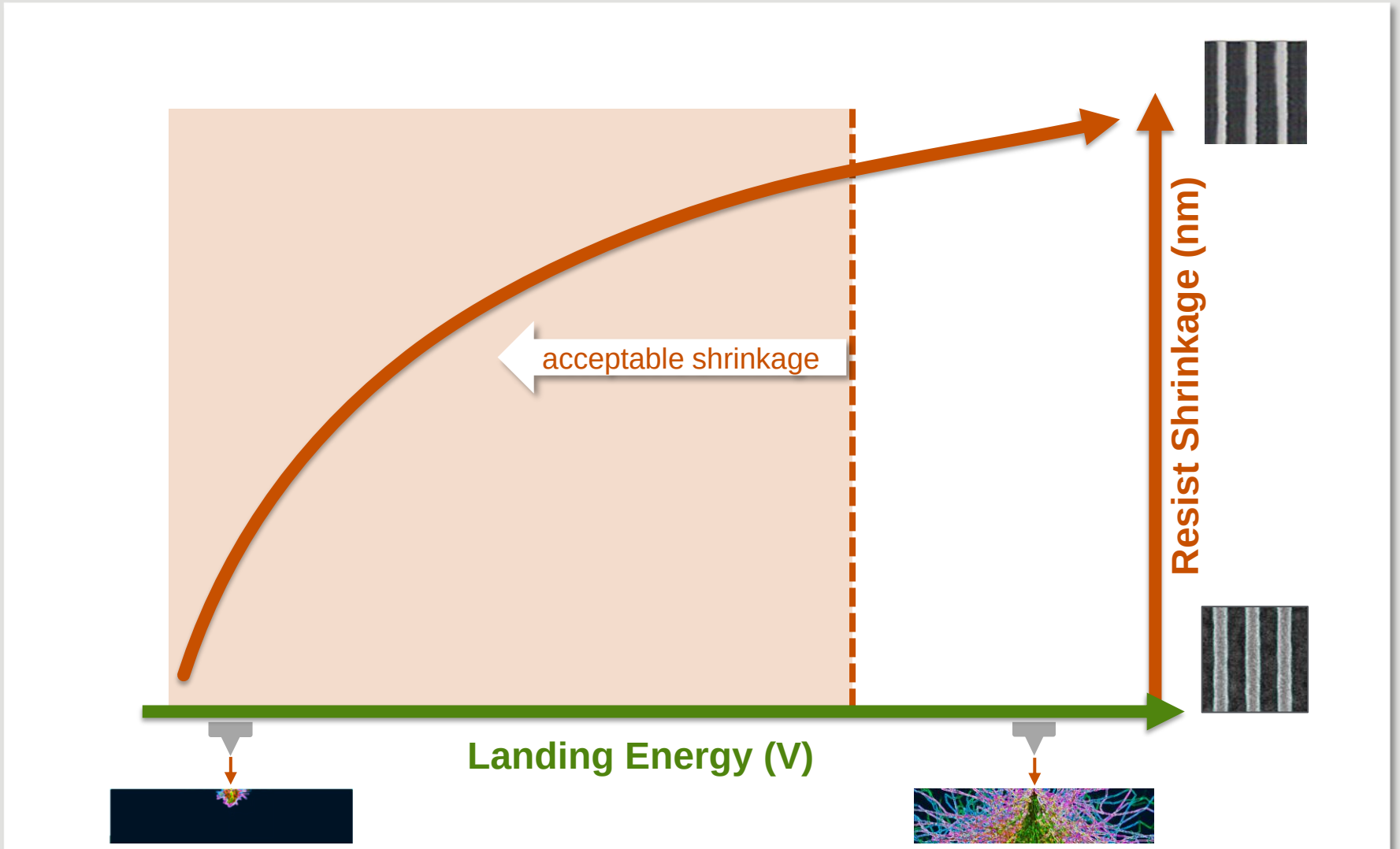


Higher Landing Energy Improves Imaging Resolution



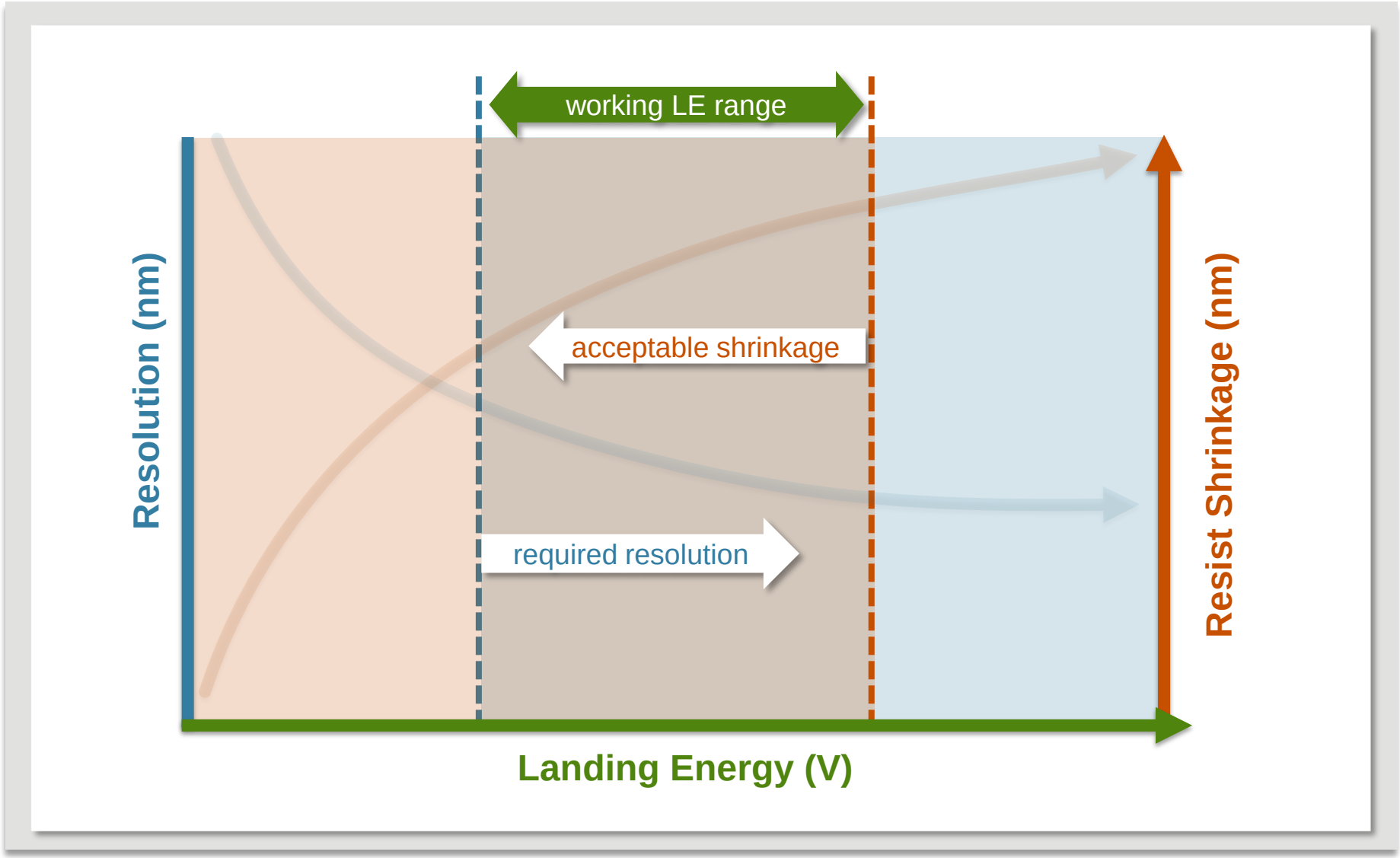
Landing energy: high energy is used to concentrate the electron beam on the target area and produce higher resolution images.

Higher Landing Energy Impacts Photoresist



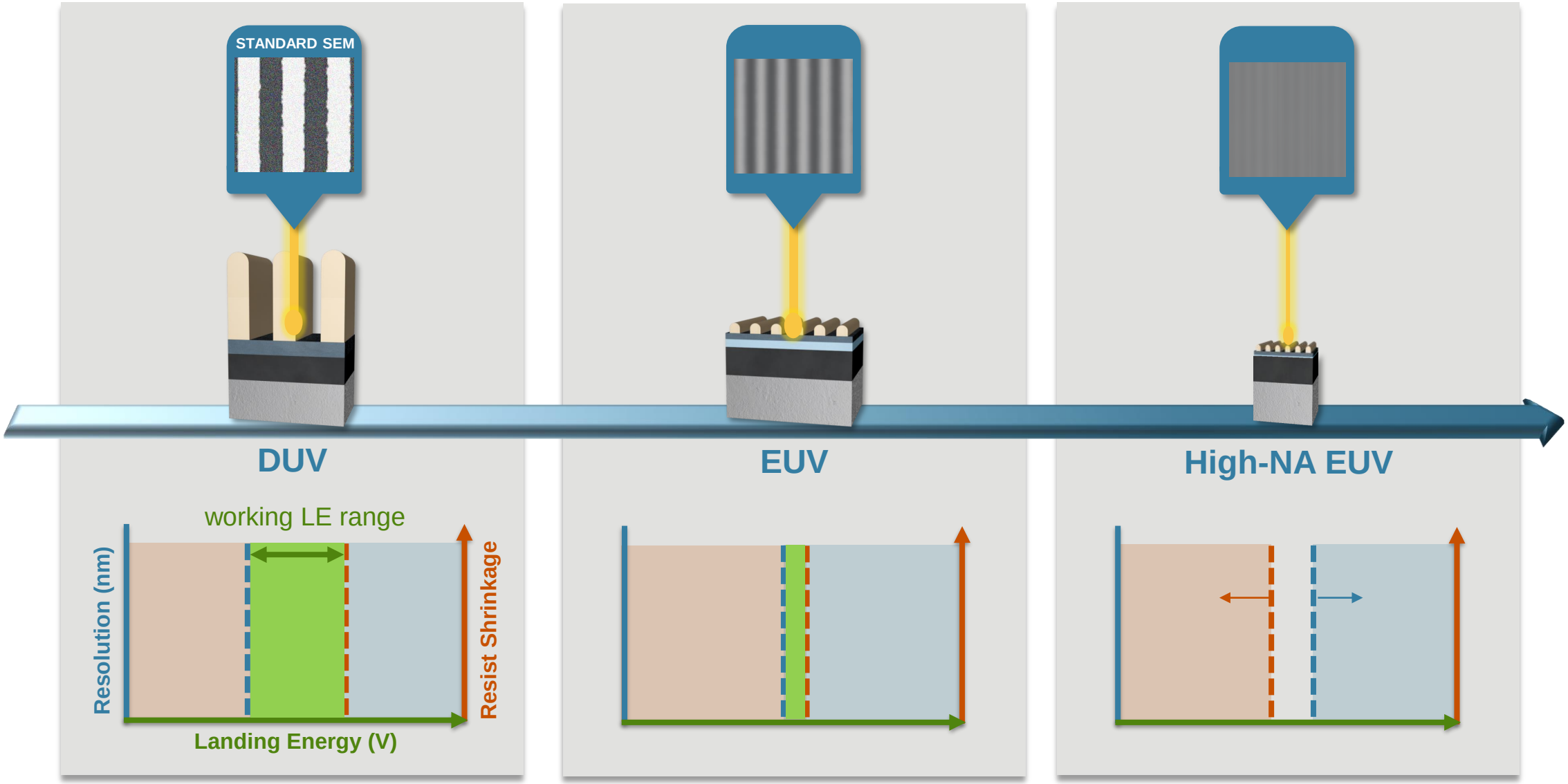
Landing energy:
High eBeam energy increases interaction with the photoresist material, resulting in excess shrinkage and pattern distortion.

Acceptable Resolution and Shrinkage Define LE Range



Working Landing Energy (LE) Range: CD-SEM landing energies that meet image resolution and shrinkage specifications, enabling lithography process control

Challenge: Working LE Range Narrows with Lithography Shrink

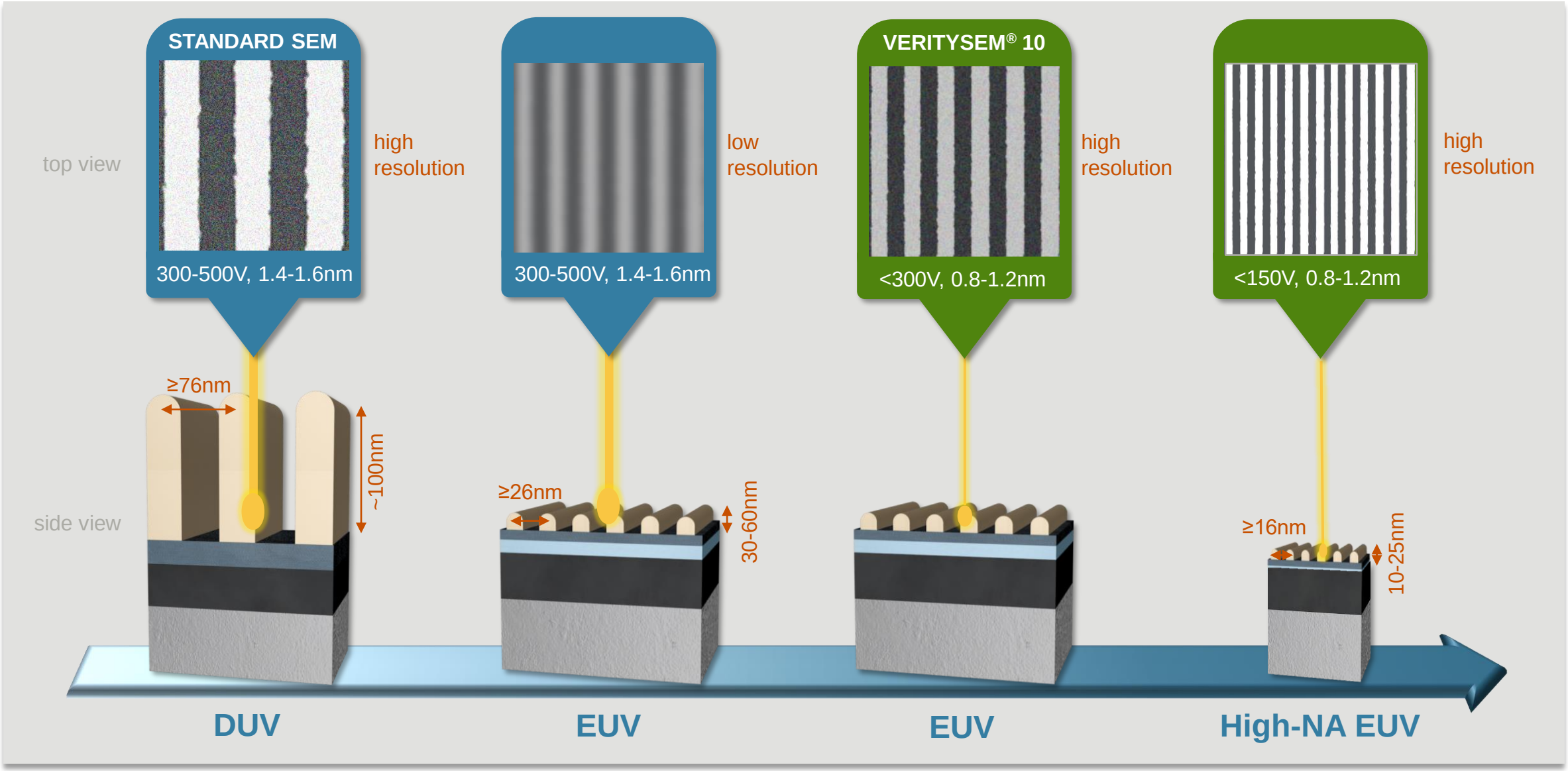


Introducing VeritySEM® 10 CD Metrology

Paving the Way to High-NA EUV

- ✓ Lower landing energy
- ✓ 2x better resolution
- ✓ Minimal resist shrinkage
- ✓ 30% faster production throughput

VeritySEM® 10 for EUV and High-NA EUV CD Metrology



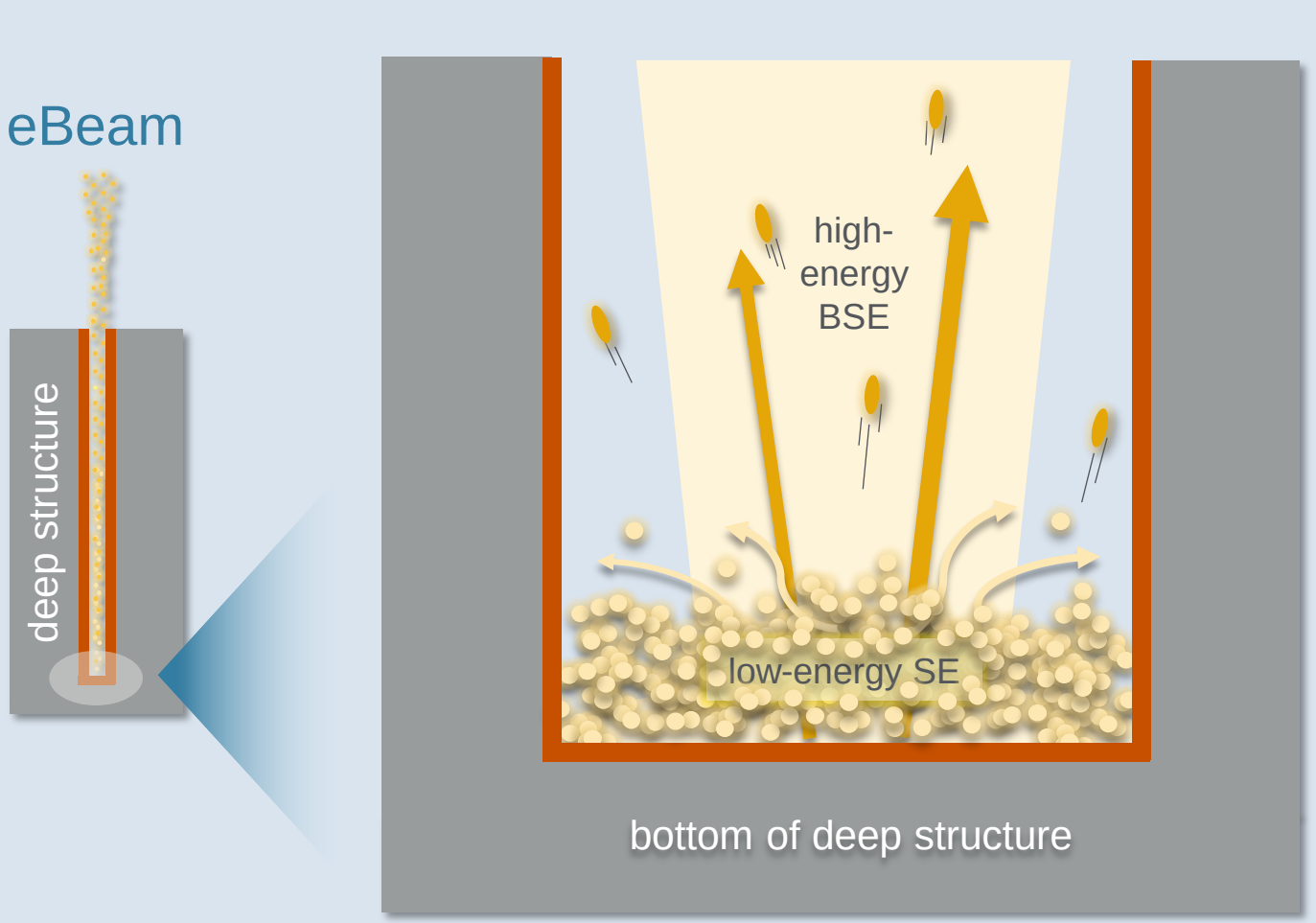
APPLIED MATERIALS

Introducing VeritySEM® 10 CD Metrology

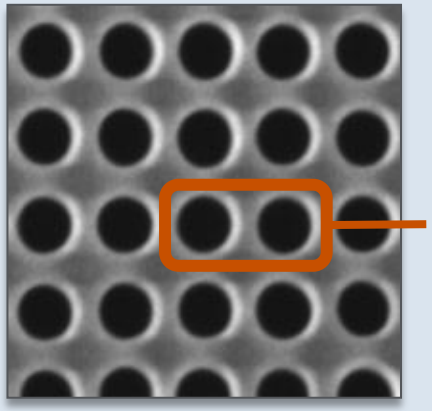
CD Metrology for 3D Structures

- ✓ GAA – 3x wider back-scattered electron collection enables epitaxy metrology
- ✓ 3D NAND – 1.5x larger field of view enables next-generation staircase metrology

Imaging 3D Structures with Back-scattered Electrons

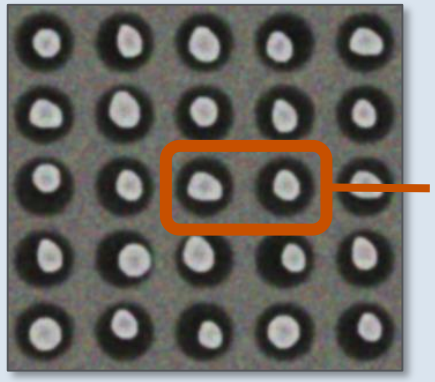


3D imaging w/ SE



cannot image deep trenches

3D imaging w/ BSE

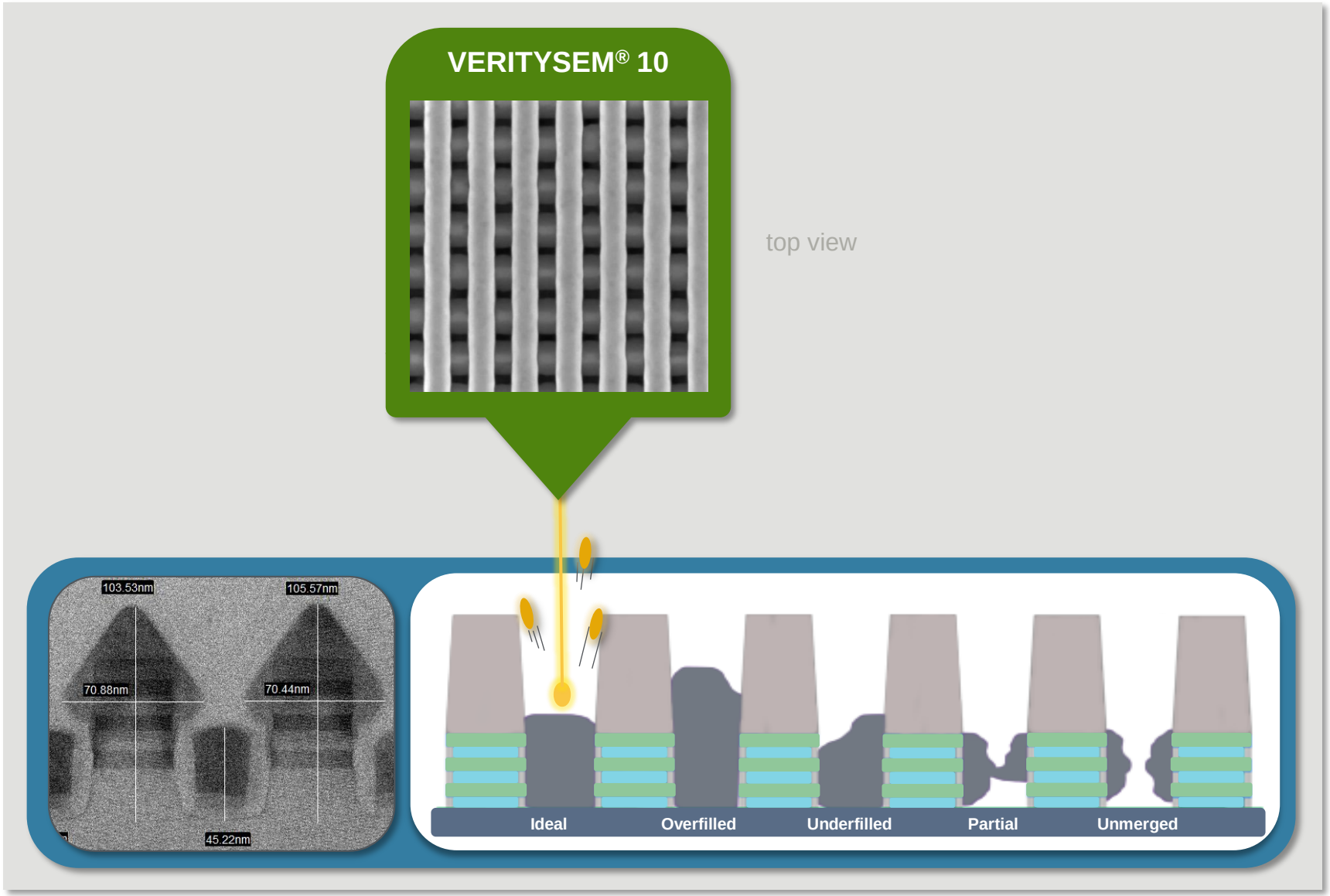


bottom of deep trenches imaged

top view

BSE: back-scattered electrons
SE: secondary electrons

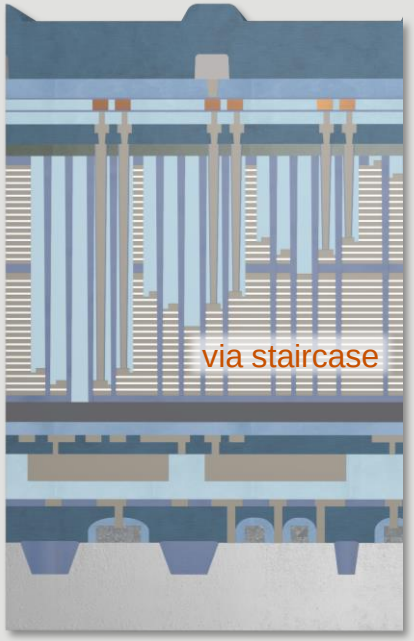
New CD Metrology Steps in GAA

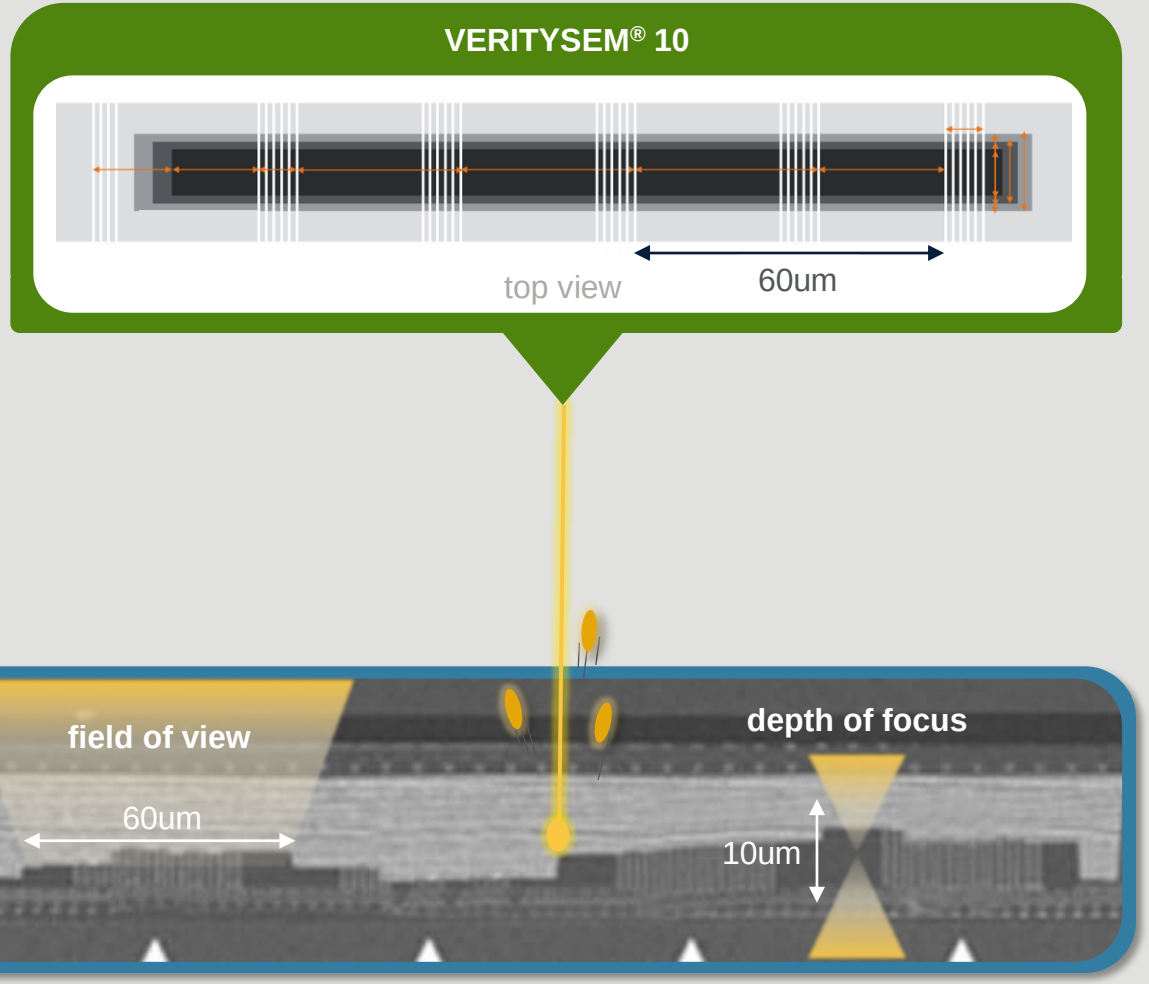


Selective epitaxy is key to GAA nanosheet engineering. VeritySEM® 10 uses BSE technology to measure and characterize the epitaxy process.

Source: Applied Materials

New CD Metrology Steps in 3D NAND





Staircase interconnect architectures increase contact density to reduce die area and cost. VeritySEM® 10 uses a large field of view with high depth of focus to measure the entire staircase structure with detailed step widths that help tune etch process recipes.

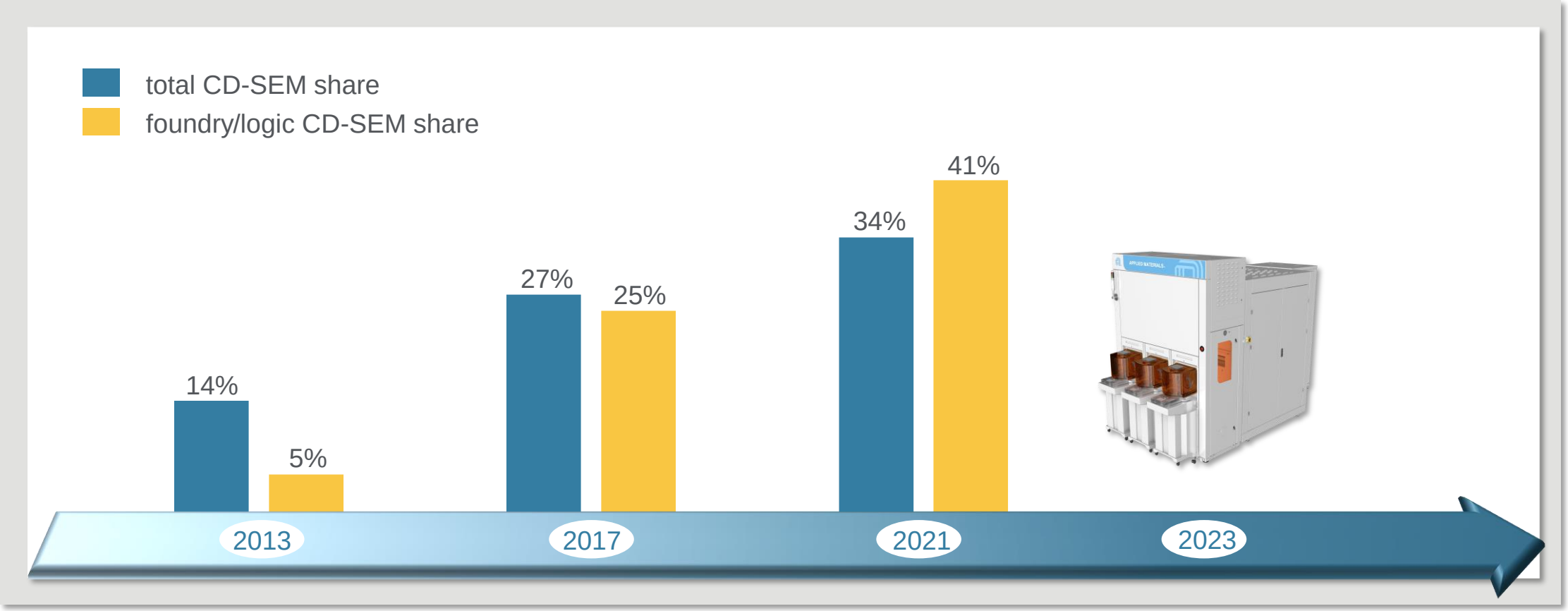
Source: Applied Materials, TechInsights

Introducing VeritySEM® 10 CD Metrology

Strong customer pull in logic and memory

- ✓ Over 30 systems shipped
- ✓ Logic: DTOR for GAA at multiple customers
- ✓ DRAM: PTOR for EUV at multiple customers
- ✓ 3D NAND: DTOR/PTOR for staircase patterning at all leading customers

>1,300 VeritySEM® Systems Shipped



Source: TechInsights

VeritySEM® 4i

VeritySEM 5i
BSE

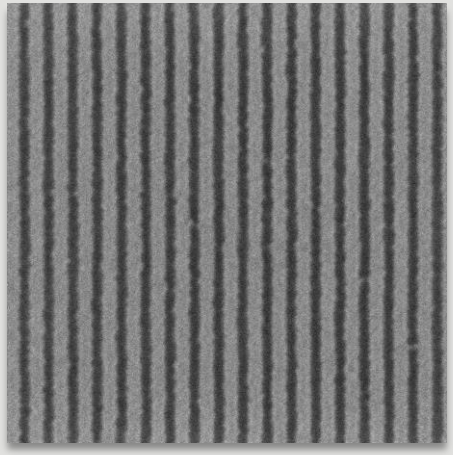
VeritySEM 6i, 7i
High Productivity

VeritySEM 10
EUV, High-NA EUV, GAA, 3D NAND

High-NA EUV Enablement: VeritySEM® 10 Papers at SPIE 2023

Title	Collaboration
Effect of Stack and **High-NA EUV** Resist Material on Shrinkage	IMEC
Unbiased Roughness Measurements for **High-NA EUV** Characterization	IMEC
Orientation Measurement on DRAM Contact Hole as an **Aberration Correlated Metric**	SK hynix
Tracing Optimized Condition for Electron Beam Metrology of **EUV Photoresist** Pattern using **Low Landing Energy In-line** Monitoring	SK hynix

High-NA EUV Pattern



VeritySEM® 10
(150V)

Source: IMEC

Q&A

APPLIED MATERIALS®

The event has concluded