# Process Control and AppliedPRO™ Master Class

PREPARED REMARKS | October 18, 2021

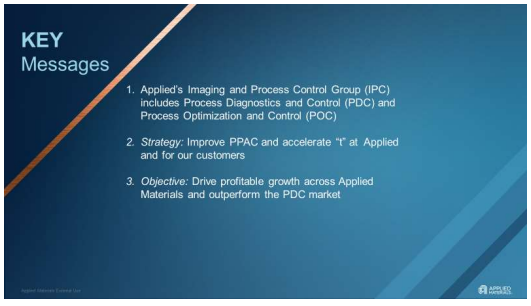
## MICHAEL SULLIVAN | Corporate Vice President, Investor Relations

Hello, everyone. I'm Mike Sullivan, head of investor relations at Applied Materials, and I'm pleased to welcome you to the fourth and final event in our 2021 Master Class series.


If you missed any of our previous events – you can still find all of the replays, slides and transcripts on the events page of our website. Today we'll cover two topics. First, process control, especially the role that patterning control plays in semiconductor manufacturing. And second, Applied's Process Recipe Optimizer – which takes advantage of big data and AI to accelerate process R&D.


And here is today's agenda. In a few moments, we'll have a fireside chat with Dan Hutcheson of VLSI Research. Next, you'll meet Keith Wells -- who's the General Manager of Applied's Imaging and Process Control group, or IPC. Keith will explain the dual mandate of our IPC organization. He'll then introduce Maayan Bar-Zvi from our Process Diagnostics and Control group based in Israel and Lior Engel, who leads our Process Optimization and Control group based in Santa Clara.

After the technology sessions, Keith will summarize our strategies and growth opportunities in process control. And then he, Maayan and Lior will all be available to take your questions.



There are three things we'd like you to know about Applied Materials and process control. One, Applied's Imaging and Process Control Group includes two distinct organizations that we'll explain today: Process Diagnostics and Control or PDC and Process Optimization and Control or POC. Two, we'd like you to know about IPC's strategy to accelerate time to market which is the "t" in PPACt at Applied and for our customers. And three, we'd like to show you how this strategy is enabling IPC's goal of helping drive profitable growth across Applied Materials while also outgrowing the PDC market.


Before we dig into the business and the technology, we wanted to give you a third-party perspective on process control. And that brings us to our fireside chat with Dan Hutcheson, who is CEO and Chairman of VLSI Research. VLSI forecasts and reports on all of the details of the wafer fab equipment industry. Dan's been in the industry for 40 years, consulting with company leaders and helping them turn technology innovations into successful businesses.

Today's Master Class will cover the techniques used in the process control industry along with roadmap and technology inflections that are continuing to change the market. Dan has been deeply involved in these changes over the years, and that makes him the perfect person to help us kick things off.

## DAN HUTCHESON | Chief Executive Officer & Chairman, VLSI Research

*Mike Sullivan:* **Dan, thank you for joining us today.**

It's my pleasure. Looking forward to it.

*Mike Sullivan:* **So, VLSI reported process control industry revenue of over $7.6 billion in 2020, which was around 12 percent of WFE. How should investors think about the role in the value of process control?**

Well, first of all, it assures value, it doesn't add value. In technology inflections, what they've done historically, is they create new yield disruptors that drive the need for more process control points that are in the process flow. That's what makes the big difference.

*Mike Sullivan:* **Right. And Dan, in today's class, we're going to be talking about inflections involving two major technologies, one optical, the other e-beam. What's a simple way to differentiate these? And why do customers use both?**

Well, the easiest way is that one uses photons to see, and the other one uses electrons. But seriously, the easiest way to think about their economic impact in the fab is around resolution and costs, which makes these core technologies really complementary to each other. Optical's low resolution makes it really quick and cheap, but blind to many things that you can't see. That's where e-beam comes in to the rescue, because it offers the extreme resolution that you need to see those things. The only problem is its slow and expensive.

*Mike Sullivan:* **Now, you've been working with companies since the 1980s. What are some of the major inflections that happened in the process control market?**

So the big one was really in the early '80s with the arrival of the stepper, and it bumped yields past the 50 percent mark, which pushed the industry from just simply culling good from bad die with tests and automated microscopes. Then the next big inflection to come after that was when optical ran out of steam as CDs continued to get smaller and smaller. And e-beam had really been waiting at the door all along, in the clean room, and it was just a matter of the CD-SEM, that was going to be this breakthrough role into the fab.

*Mike Sullivan:* **Got it. And when you think about the industry today, what are some of the major inflections that are affecting the roadmap?**

Well, it's back to the future again. As lithography moves into this new EUV era, it's all about ensuring that overlay is still working. And we've got this problem between after develop and then after etch, it's no longer the sure thing that it once was. And so now, everyone seems to be having problems with yield at 3N. And I'm going to use 3N because nanometers just doesn't make sense anymore. So one of the biggest problems that engineers are having today is the correlation and overlay between develop and etch that's inside the die itself. And what happens is there's a lot of mush of uncertainty that's happening, that's being created by intra-die stress, and it's really not seen in the overlay marks because they're just so huge. It's kind of like the Apple commercial, where he's trying to find a phone in the haystack. He needs a tool and in the Apple commercial he has a watch to find it. But in this case, the overlay marks are really the haystack. And the tool that you need is something, like say, Applied Materials PROVision to find it. And that allows you to look inside the die and actually see what the overlay is, and get the kind of precision you need. And so, as a result, we're seeing all these new problems just kind of crop up because of EUV kind of breaking the log jam and that's just the way it goes.

*Mike Sullivan:* **Right. So now, when you talk to the chip makers, what are they saying about AI when it comes to manufacturing?**

That's interesting, because that's where the, "if you can find it you can control it," comes in. Everyone's finding innovative new ways to use AI. Automatic entrance doors, for example: in the store you go to, they now have AI vision control for safety. And when it comes to the wafer fab, the potential is just enormous, as Gary Dickerson has pointed out so far, really too numerous to address here. I do see three fundamental stumbling blocks for chipmakers trying to implement AI in the fab. The first one is the internal turf wars that occur between IT, that reports to finance in their organization, to what's really needed to be done in the fab. And then the second one is when they find something, they still need to

make it actionable. And they can't do that without the equipment makers' partnership that you're working with. And then the third is it's really hard to get big enough data in a single fab. An equipment supplier has some level of access to every tool and every chamber that's ever been installed, and a wafer fab could only have a subset of this. So the differentiator becomes a question of if the data set is big enough to really provide useful answers.

*Mike Sullivan:* **Okay, that makes sense. And then when you think about AI and process control, what should companies like Applied Materials be doing to add value?**

Yes, you see, anybody can do AI, but it's actionability that makes AI valuable. If it's not actionable, it's just intelligence that's artificial and not so interesting. They have tools and they have the installed base to understand how to fix the problem.

*Mike Sullivan:* **And then shifting gears, Applied and our customers are really focused on driving power, performance, area cost and time to market. Do you see any relationships between process control and P-PACT?**

Absolutely. Variability makes chip run slower or consume more power. This lowers the price of the chip. It also forces designers to spread things apart, and that increases the die size. And once you increase the die size, that increases your cost. And so the hidden P takes a hit. And the question is, you might ask, "Well, what's the heck's the hidden P?" It's profitability. If your price is going down, your cost is going up, you're losing money.

*Mike Sullivan:* **That makes sense. So now let me ask a provocative question. With the AI getting better every year, are we still going to need process control engineers, say five to 10 years into the future?**

Of course we will. Fab managers were once fearful of putting computers in a fab for this reason, and look what happened to those who resisted the technology: they all got retired. In reality, AI is just a new tool in the engineer's toolbox. Artificial intelligence will always need real intelligence to guide it at the cutting edge.

*Mike Sullivan:* **Finally Dan, later in the class, we'll talk about using AI to perfect the process recipes. Do you think we'll get to the point where we need a lot less process control equipment?**

Well, that's a definitely a provocative question, and the history has shown: no. What we've traditionally needed is more and more process control. And that's because we keep pushing technology and we keep finding new inflections, new problems to solve. And that means we need new tools to really identify with those problems on an ongoing basis in the fab. So I just can't wait to see the next inflection.

*Mike Sullivan:* **Well, thank you Dan for your answers and for being here today.**

It's my pleasure.

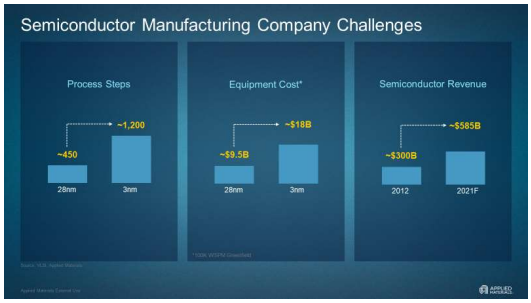
*Mike Sullivan:* **Keith, it's over to you.**

## KEITH WELLS | Group Vice President, GM, Imaging and Process Control

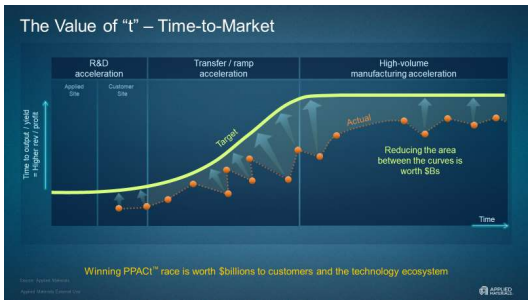
Thanks Mike.

I'm very pleased to be here today to introduce you to Applied's Imaging and Process Control Group. And to introduce two of my colleagues who will show you how the industry is going through some major inflections.

Let me give you a little of my own background as well. I'm a physicist by training, and early in my career, I joined a company called Tencor Instruments which went on to merge with another company called KLA. In my 27 years there, I developed foundational technologies in areas like imaging, sensors, computing and algorithms. I also served as general manager of the eBeam division and later the General Manager of Optical Inspection Division. Along the way, I had the opportunity to work with some people you may know, including Gary Dickerson and Ali Salehpour. Last year I jumped at the chance to join Applied and lead IPC.

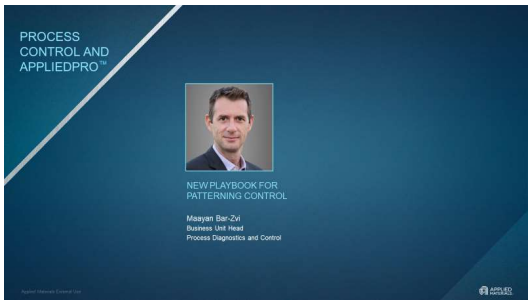



Today, we're in a very important time in the process control industry because our customers have never faced so many pressures. First, complexity is increasing. The number of logic process steps has tripled since the 2D transistor era. And we're moving to more complex structures like Gate All Around. Second, the cost to compete has risen dramatically. The equipment cost of a large 3-nanometer fab is approaching $20 billion dollars – which is twice the cost of a fab at the 28 nanometer node. And third, the semiconductor markets are bigger and more valuable than ever. Being first to market with the best server or AI chip is worth billions to chipmakers -- and especially to cloud data center companies which are now the most valuable companies in the world.



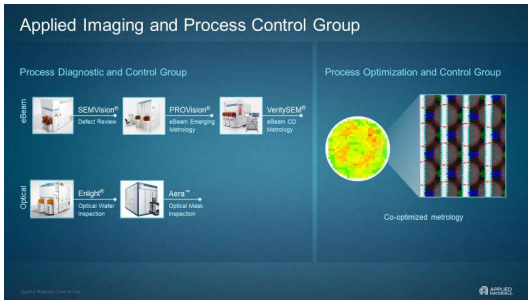

What this means is that time to yield is worth billions in revenue and profitability over the life of a new node. It directly impacts our customers' market share, revenue and ROIC. With that context, I'll now introduce you to the two major groups within our IPC business -- and introduce our Master Class topics and presenters.


Applied IPC has two major parts: first, Process Diagnostics and Control, or PDC. Our goal is to grow in the market by delivering cutting-edge inspection and metrology systems -- using both optical and eBeam technologies -- to serve the world's leading customers. Within the PDC industry, we're second in overall revenue, and number one in eBeam revenue.

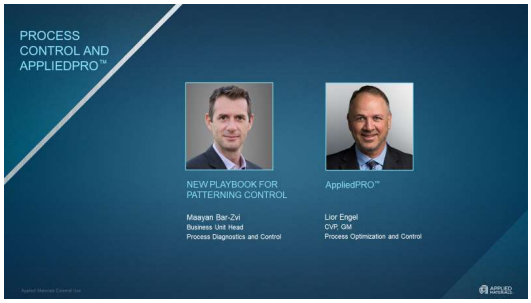



Maayan Bar-Zvi works in our PDC group in Israel. Maayan studied engineering at Tel-Aviv University, and today he is the head of our patterning division. He'll show you how increasing semiconductor process complexity is creating a major technology inflection. The optical metrology tools we've always relied on, now have some serious measurement gaps -- or blind spots -- that impact time to market and yield. Maayan will introduce a new playbook for patterning control that is creating strong customer pull for Applied's eBeam technology.

He'll introduce you to our newest PDC product, PROVision 3E, which is growing rapidly as customers add new eBeam steps. These inflections are driving record sales for PDC as I'll discuss in my summary later today.




Second, we have our Process Optimization and Control group, or POC. It's a new and very unique organization. We co-optimize process recipes, metrology techniques, and advanced analytics including AI. We partner with Applied's business units and our customers to accelerate R&D and expand process windows.




You'll meet Lior Engel -- who is general manager of our Process Optimization and Control group. Lior has two degrees in physics from leading universities in Israel along with a business degree from Boston University. He has more than 25 years of experience in the process control industry. And he'll show you how we're developing optimal process recipes -- and delivering them to customers -- with a dedicated global field team of experts.

POC is helping Applied gain share in areas like CVD and etch -- where co-optimization and holistic solutions enable our customers to accelerate R&D and ramp. After the presentations, I'll show you how these technologies are driving growth in our business and changes to the Process Control industry's spending mix. Then we will be available to answer your questions.

So thank you for joining us.

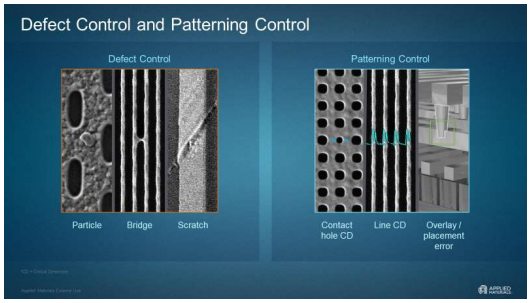
And now, Maayan, over to you.

## MAAYAN BAR-ZVI | Business Unit Head, Process Diagnostics and Control

Thank you, Keith.

It's a pleasure to join you today. As Keith said, I work at Applied's Imaging and Process Control group in Rehovot Israel, and I've been with Applied for 18 years. Today I manage our patterning products – both our CDSEM – which is called VeritySEM – and PROVision, which is in the heart of today's presentation.

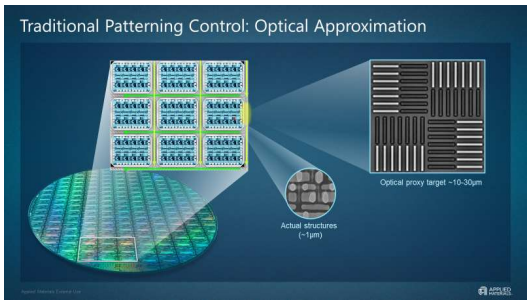

I have several goals for today's Master Class: One, I will explain the critical role that patterning control plays in semiconductor manufacturing. Two, I'll help you see that we're reaching an inflection point -- where the traditional, optical methods of patterning control are no longer enough for our customers. Three, I will introduce a "new playbook" for patterning control that our customers are now adopting. And Four, I will introduce a new product called PROVision 3E that is designed for the new playbook.




First, patterning control is not the same as defect control, which we discussed in March when we launched our new Enlight optical wafer inspection system with ExtractAI technology. That was all about inspection: finding and controlling yield-killing defects on the wafer such as particles, bridges and scratches. Instead, patterning control is about creating the right patterns on each successive layer that makes up a chip. This is about metrology, which is the scientific study of measurement. Each layer of the chip is made up of features like lines, spaces and holes.

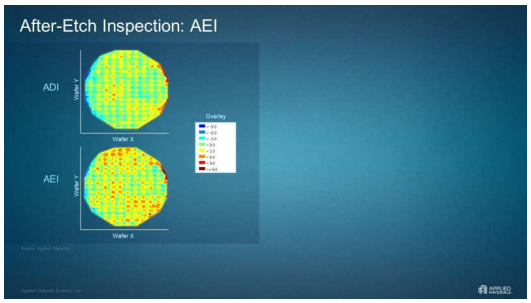
The layers are stacked up, one after another. And if they're patterned correctly, they'll produce working transistors and interconnects. With each layer, we need to do two things: One, make sure the critical dimensions of the features are correct. This is called CD control, and it typically uses eBeam technology like our VeritySEM.

Two, we need to make sure the features on each new layer of the chip align perfectly with the opposite features on the layer beneath. This is often called overlay control by generalists. People in the field use a more precise term which is called placement. Traditionally, optical tools were adequate for this. I will introduce you to technology inflections that are creating strong customer pull for what we call “Emerging SEM Metrology.”

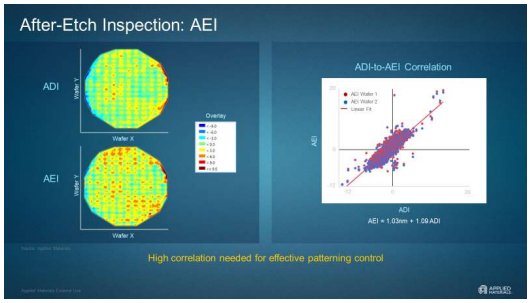



Let’s start by reviewing patterning control using the traditional playbook. In manufacturing each new layer of a chip, the wafer is coated with photoresist. The litho tool holds a photomask that has the desired pattern, and as light shines through the mask, the die patterns are exposed onto the resist. Around each die there are nonfunctional areas that we call scribe lines or streets which are eventually removed when the wafer is diced. Importantly, these areas include “proxy targets” which are vertical and horizontal marks that help optical metrology tools estimate whether the patterns in each die are placed correctly.

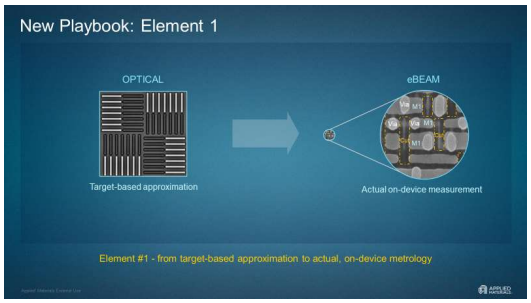

After lithography, we come to an important decision point: Either remove the photoresist and rework the pattern or commit to etching the new pattern into the expensive wafer. To help decide, an important metrology step called after-development inspection -- or “ADI” -- is performed. Overlay ADI is traditionally performed by optical metrology tools. They use the “targets” in the scribe lines as a guide. And they use advanced algorithms to approximate whether the placement is correct. This slide shows the kinds of data process engineers receive from ADI to help make the critical decision of whether to etch or rework the pattern. If the ADI looks good, the pattern is etched.




And this brings us to a second overlay metrology step called after-etch inspection – or “AEI.” Now we can directly measure whether the etch resulted in features with the right placement. This slide demonstrates AEI data. Process control engineers need the ADI and AEI data to be very well correlated and unbiased.

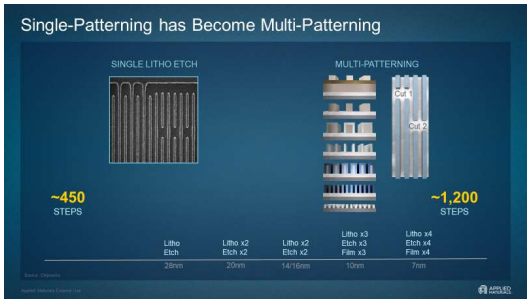



This traditional playbook for patterning control was developed during the single patterning era when each layer was patterned using one mask and one etch. Every couple years, we reduced the X and y dimensions to deliver twice the number of transistors per die size. The ADI and AEI data were highly correlated, and the shrinks proceeded like clockwork. Now let’s talk about the growing need for a new playbook. After many generations of 2D shrinking, the on-die features are about 10 times smaller than the optical targets. As a result, the ADI measurements are becoming uncorrelated with AEI results.

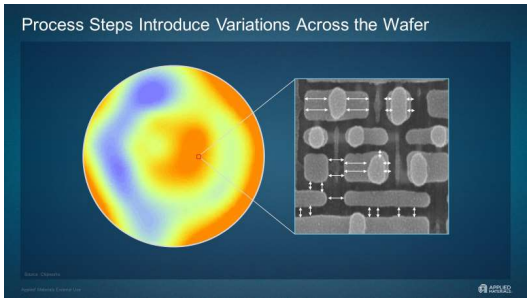



This creates issues for engineers working to create a healthy process technology. Put simply, you can't fix what you can't measure. And you can't measure what you can't see. And this is why customers are now supplementing optical metrology with eBeam overlay. The advantage of eBeam technology is that it has nanometer resolution. This allows our customers to see, measure and fix placement issues that are below the resolution of optical metrology.

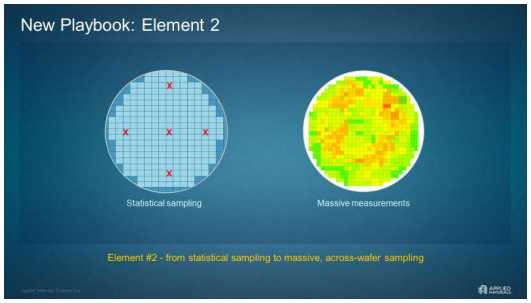
And this brings us to Element 1 of the new playbook for patterning control. It is the transition from target-based approximation of patterns using optical technology to actual, on device metrology using eBeam. Today, customers are using eBeam for overlay AEI because it gives them the ground truth of what is being patterned on the wafer. In the future, they will use eBeam for both AEI and ADI. This will give them one set of highly correlated data that can provide tight control loops between all their process and patterning steps.



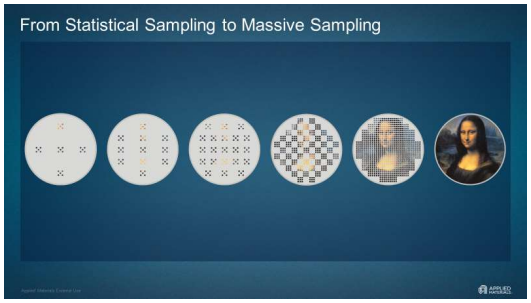

Now let's discuss element two of the new playbook. You probably know that we've gone well beyond the single-patterning era where a single deposition and etch are used to create the smallest patterns. Today we use multi-patterning, where one litho step is followed by two or even four deposition and etch steps to create the smallest lines and spaces. Even EUV patterning is moving to double patterning. And each step adds pattern variability.



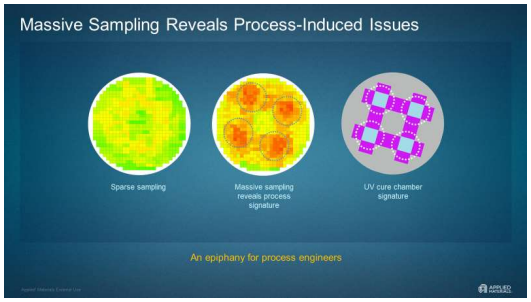

What's important to understand is that process conditions are slightly different in different regions of the wafers. This means the pattern of each die being formed will be slightly different depending on where the die sits on the wafer. Also, new materials behave in new ways. These variations are difficult to detect and control using technology that was designed during the single-patterning era.



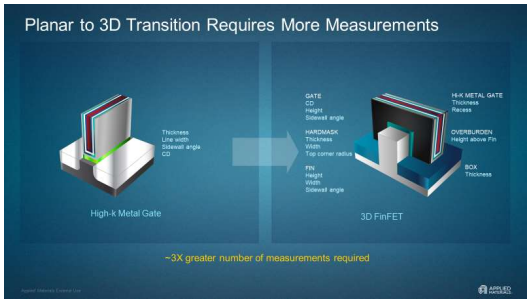

And this brings us to element 2 of the new playbook for patterning control which is the transition from statistical sampling of a small number of dies to massive across-wafer sampling.



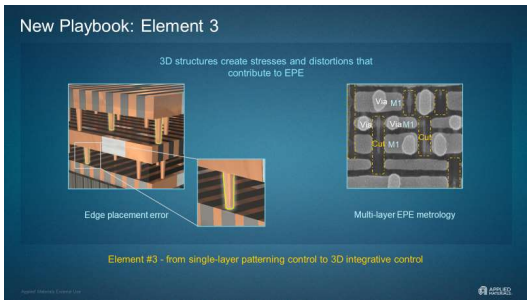

Let's illustrate how massive, across-wafer sampling can reveal patterns. Here is a small number of data points similar to the statistical die sampling used in optical overlay. You cannot notice any across-wafer variability issues. Now let's give you more samples. Thanks to the additional data, it is now clear to you that this is the Mona Lisa.



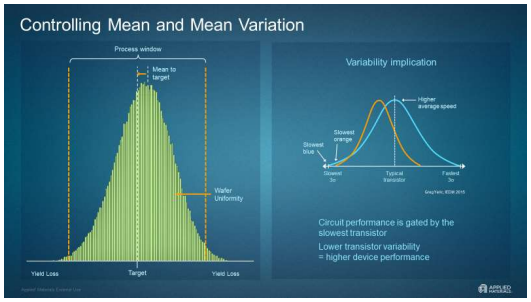

In the same way, massive across-wafer sampling reveals process-induced patterning issues. Here, increased sampling shows a process engineer that she has a pattern variation issue related to annealing a particular film on the wafer. This epiphany can be used to adjust the anneal process recipe -- to increase across-wafer uniformity and die yield.



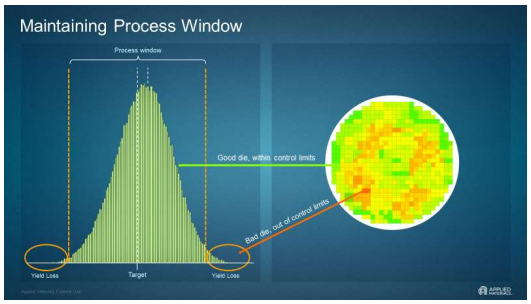

Now let's discuss the third and final element of the new playbook. You probably know that we have reached the limits of planar, 2D transistor shrinking. 3D designs like FinFETs have taller features and higher aspect ratios. Due to their complexity, 3D FinFETs can require three times the number of measurements as compared to planar. And Gate All Around transistors will require even more metrology. In addition, 3D structures can create stresses and distortions -- locally, across the wafer, and between layers.




Element 3 of the new playbook is the transition from single-layer patterning control to 3D integrative control. It calls for more metrology within and between layers; larger, multidimensional data sets; and AI pattern recognition.

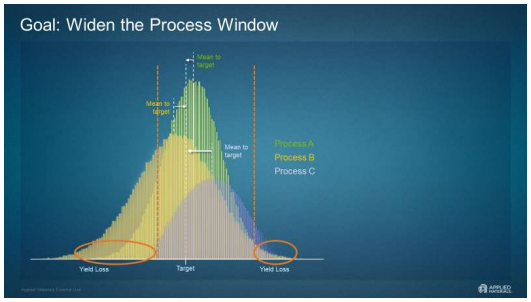



Now, before I introduce PROVision 3E let me give you some additional background on the science of patterning control. This will help you understand how PROVision can help our customers -- and it will help you later when Lior discusses POC. First, if engineers can tune their processes to get the mean of pattern variation as close as possible to the center of the ideal distribution, they can achieve the best chip performance and power efficiency. This is because performance and power degrade as we drift away from the optimum, and because a circuit's overall performance is gated by its slowest component.

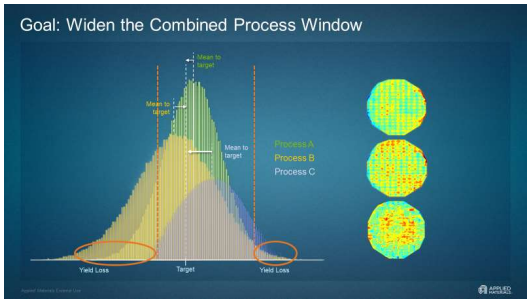



Also, if the variation falls outside of what we call the "process window," there can be malfunctions and yield loss. So, there are three key objectives for patterning process control: One, maintain the mean of the histogram as close as possible to the target value. This requires basic sampling. Two, minimize the distribution around the mean. Achieving tight distributions, uniformly across the entire wafer, is more difficult especially as we use multi-patterning, new materials and 3D structures. Three, widen the process window.

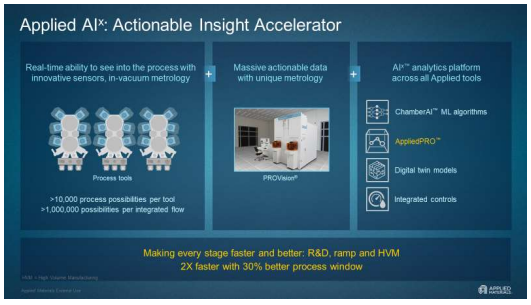
I'll explain. Manufacturing process steps can have many variables such as materials composition and purity, temperature, pressure, energy and time. And a number of process steps are used in a sequence to complete each layer of the chip. If we can find the parameters across all of these variables and steps that give us the widest possible process window, then we can have the highest yields in production. And each percentage of yield goes directly to gross margin.




Let's look at a histogram that captures the complexity. There is a distribution for each process step. And achieving the widest process window means increasing the control of the mean and distribution of each one. As you can imagine, this requires massive amounts of data, which we call "big in-line data."



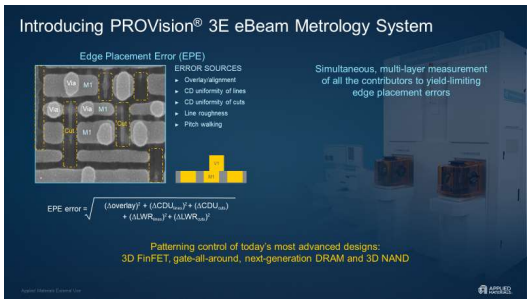

It also requires massive analytics. And by now you can probably guess that the biggest breakthroughs are possible with machine learning and artificial intelligence. Our AIx™ platform is designed to help produce the data and "actionable insights" engineers need to accelerate R&D and widen process windows.




As Lior will demonstrate, this new approach is highly enabling. We can model materials, chemistry, and physics to predict what will happen even before we process wafers. We can use digital twins to compare systems and chambers to their optimums and dial in their settings. Using sensors, we can see into processes and gather data as the materials are being modified. And using eBeam metrology, we can measure the on-wafer results at millions of different locations, with nanometer resolution and in more than one layer at the same time. This is the future of process and patterning control.

And now I'm pleased to introduce PROVision 3E, which we are officially launching today. In fact, we started shipping PROVision 3E to customers last year, in foundry-logic, DRAM and NAND. And today, we already have over 30 systems in the field.


I'll introduce you to the key features and benefits. PROVision 3E uses our industry-leading eBeam technology, which is why we have the number-one position in eBeam review. PROVision 3E also includes the CD metrology capabilities we developed in our VeritySEM family, which is rapidly gaining share. And very importantly, PROVision 3E is designed for speed. The E in 3E stands for "Elluminator," which is our technology for seeing deeply into layers and structures. We bounce electrons off the structures and collect them as they return to the system. These "back-scattered electrons" allow us to see hundreds of nanometers deep enabling us to measure placement and critical dimensions in as many as 20 layers. Compared to the previous version, PROVision 3E has higher energy, which improves deep structure imaging by 50 percent. And while PROVision is powerful, it doesn't damage the fragile structures our customers are creating.




It simultaneously measures all of the contributors to edge placement errors, including overlay errors, CD uniformity, and line width roughness. It gives engineers the data they need to refine process recipes for a wide range of equipment from litho to etch, deposition, anneals and CMP. PROVision 3E is designed to help customers with the most challenging patterning jobs today, including 3-nanometer foundry-logic, Gate-All-Around, DRAM at the 1a node and beyond, and 3D NAND stacks of 120 layers and more.


Relating back to the new patterning control playbook, PROVision 3E helps customers accelerate the transition: first, from target-based approximation to actual, on device metrology; second, from statistical sampling to massive across-wafer sampling; and third, from single-layer control to 3D integrative control.

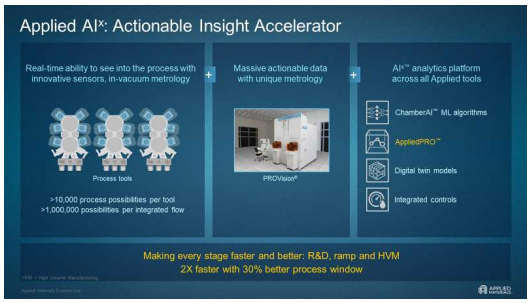
I hope you enjoyed learning more about manufacturing and patterning control, the new playbook, and PROVision 3E.

Now I'd like to invite Lior to discuss process recipe optimization. Lior?

## LIOR ENGEL | Corporate Vice President , GM, Process Optimization and Control

Thank you Maayan.

Hello, I am Lior Engel, General Manager of POC, the Process Optimization and Control group that Keith introduced earlier.



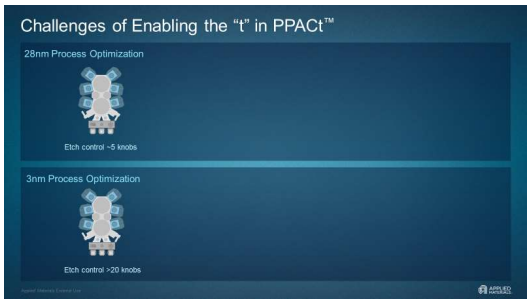

Let me start with a brief overview of AIx, our Actionable Insight Accelerator, that we introduced at our investor meeting in April. AIx combines process technology, sensors, metrology, and data analytics into a platform that accelerates every step of the journey from R&D to ramp and high-volume manufacturing. AIx delivers better and faster insights to process engineers both at Applied and at our customers. This accelerates time to market, which is the "t" in PPACt™.

Referring to the left side of the slide, we've designed hundreds of sensors into our process chambers so that we can collect data about all the variables. We've also put metrology into our deposition

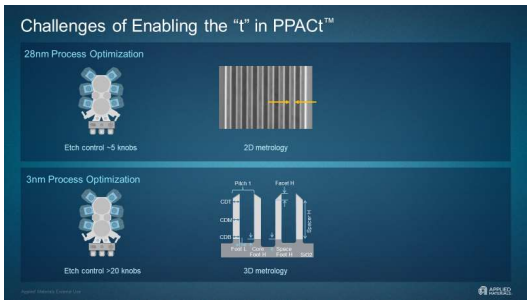
systems so we can measure the quality and thickness of films as they are being created in vacuum. Every process tool has many process knobs, like gas flow and temperature, which are used to create recipes. There can be over 10 thousand combinations in a unit process recipe and over 1 million combinations in an integrated process flow. I'll address this in a moment.

In the middle, we use PROVision® to measure what happens on the wafer as a result of these combinations. And on the right, we use our AIx analytical tools to predict and measure which process variables deliver the best on-wafer results. Our goal is to accelerate R&D by 2X and widen process windows by 30 percent. In the next few minutes, I'll walk you through the unique metrology we have developed using PROVision. And I'll illustrate AppliedPRO™, our process recipe optimizer.

So, what are challenges we solved with PROVision and AppliedPRO? It is the "t" in PPACt. The time it takes to optimize a process tool recipe that will meet customers' requirements. For example, we may help them optimize processes to create more uniform lines and spaces in multi-patterning. Also, we may help them adopt new CVD hardmask films and etch recipes that improve the patterning of DRAM capacitors and 3D NAND memory holes. We are using our technology to optimize other steps as well, including selective deposition, selective removal and Integrated Materials Solutions or IMS.

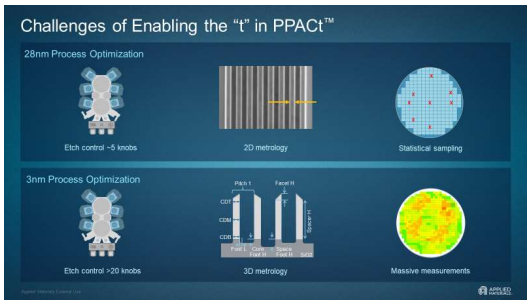



Process recipe optimization has three growing challenges. One, the number of process knobs is increasing. Knobs can include gas flow, pressure, energy, temperature and time. The number of knobs is increasing node over node as process tool requirements become more demanding. Here, we show you how the number of key etch knobs has increased from just a handful at 28 nanometers to over 20 today.

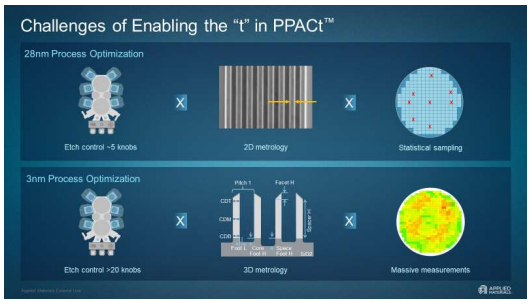



The second challenge is the transition from 2D to 3D structures. In the earlier days of the industry, process engineers mainly needed to optimize the width of the lines from a tops-down perspective, as

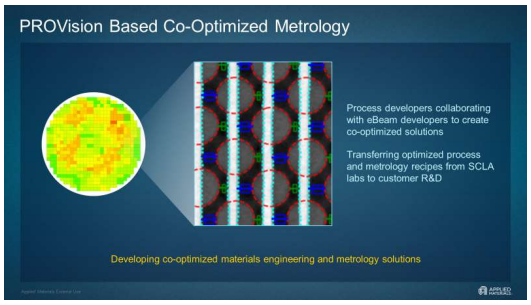
shown in the upper middle diagram. Today, process engineers need to tune structures across the X, Y and Z axis controlling dimensions like bottom CD, footing, recess and more.




The third challenge is that engineers need to meet these tight specifications in all of the structures, uniformly across the entire wafer. On the right, you see how massive measurements can reveal subtle process variations that we call "signatures."



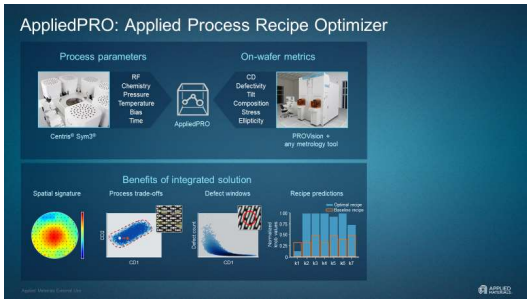

So, engineers have to deal with more knobs to control 3D structures and reduce variability across the entire wafer. What the engineer wants to know is: which knob or combination of knobs will produce the best devices and the widest process window. Solving this multi-dimensional optimization challenge is the key to faster time to market. To accelerate PPACt, our POC group is working in two directions. This first direction is what we call "co-optimized metrology."



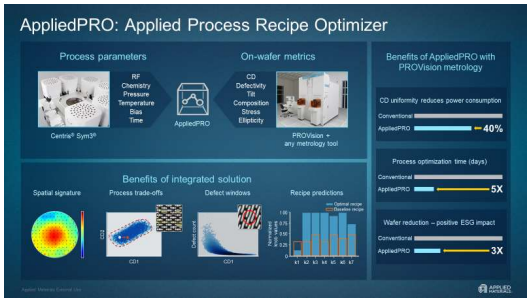

Here, Applied's process developers collaborate with our eBeam metrology developers to create co-optimized materials engineering and metrology solutions. The teams work on specific layers that are the most critical for our customers to perfect in order to complete their most advanced nodes. Once we

qualify an optimized recipe in our own labs we quickly export it to a customer's R&D site and eventually their high-volume manufacturing sites.

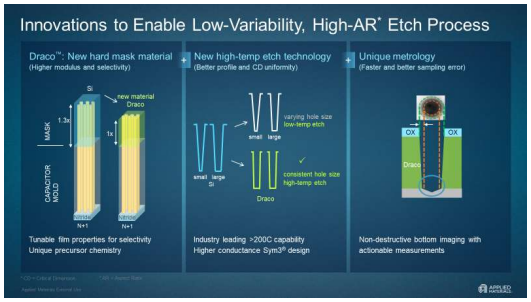
In the field, we install the process and metrology recipes so that we and our customers can hit the ground running, accelerating the "t." This chart demonstrates our co-optimized metrology using PROVision. Our customers receive massive, on device, across-wafer measurements of critical features in multiple layers with nanometer resolution. This data is unique and highly enabling.



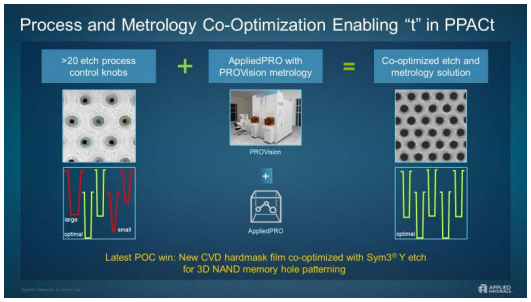

The second direction our POC group is driving is called AppliedPRO which stands for Applied Process Recipe Optimizer. Here we are using advanced analytics to create a multidimensional solution space. It correlates the process knobs inputs and the massive, on-wafer measurements. The process engineers work in an intuitive visualization environment where they can tailor process optimizations to solve R&D challenges better and faster. AppliedPRO delivers three very important benefits to our customers who are in a race against time.




First, we help customers predict and quickly dial in the most optimized recipes for specific PPACt outcomes. Second, we enable them to do this with the fewest physical experiments, saving R&D cycle time. And, third, we accomplish this using the fewest number of R&D wafers, which are precious resources. So AppliedPRO delivers the best outcomes in the shortest time, at the lowest possible cost. And since customers are developing multiple critical layers at the same time, AppliedPRO can have a multiplier effect on R&D acceleration.




Let me give you an example of how the POC group helps drive growth at Applied Materials. At the Memory Master Class we showed how we are using AppliedPRO to accelerate DRAM capacitor patterning recipes based on a new film called Draco. This has created a billion-dollar growth opportunity for us, notably in CVD and etch. It's also helping fuel our growth in eBeam.




This slide summarizes our most recent POC win, which is a critical 3D NAND patterning layer. Here, we've co-optimized a new CVD film with a new member of the Sym3 family and PROVision3E. This year, we have 25 AppliedPRO engagements in DRAM, NAND and foundry-logic. These are giving us new ways to work more closely with our customers in R&D, ramp and high-volume manufacturing including in our services business. Next year, we plan to have 50 AppliedPRO engagements.

In summary, I hope you enjoyed learning more about the process challenges our customers are facing and how we are helping them with AppliedPRO which is a major component of our AIx platform. And now, I would like to pass the meeting back to Keith.

Keith?

## KEITH WELLS | Group Vice President, GM, Imaging and Process Control

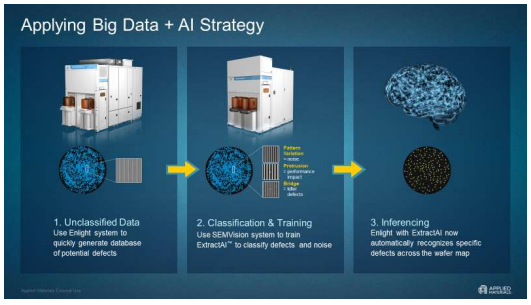
Thank you, Lior and Mayan.

Now I'd like to summarize some of the key takeaways from the Master Class and share our growth expectations. Earlier I explained that Applied's IPC group has two major parts.

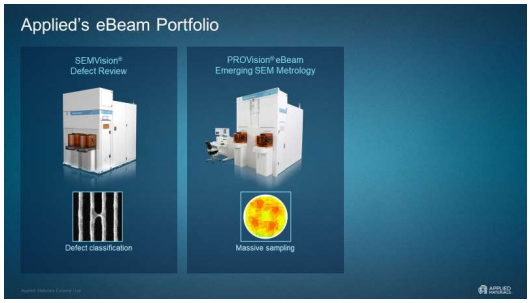

As you saw from Lior, our POC group is complementing Applied's unique breadth and depth with eBeam metrology and advanced analytics to give us an edge in process equipment optimization. This enables us to accelerate R&D within Applied from unit process to co-optimized and integrated solutions. We offer these proven solutions to our customers where they can accelerate the “t” in PPACt from R&D to ramp and high-volume manufacturing. In our PDC business, we're using optical and eBeam technologies to deliver cutting edge inspection and metrology systems. We aim to grow faster than the market and contribute strong profitability to Applied's Semiconductor Systems reporting segment.

From Maayan you saw that major inflections are happening in the industry, which are increasing the market for eBeam technology. This is creating strong customer pull for PROVision and helping Applied PDC grow faster than the market.

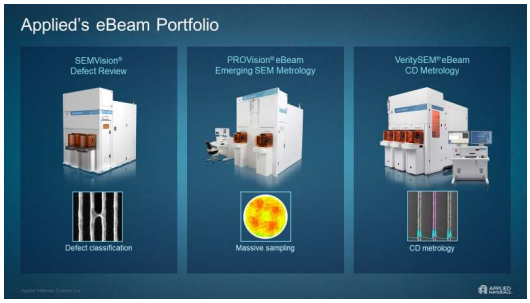

I'll take a moment to summarize the three major products in our eBeam portfolio. First SEMVision is our eBeam review system used in patterned and bear wafer inspection. It complements optical inspection systems, giving process engineers a sub-nanometer look at yield-killing defects that optical inspection tools can detect, but not actually resolve and classify.



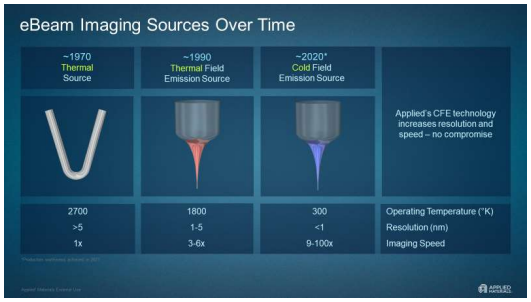
As we discussed in March, we use our optical inspection system called Enlight to quickly scan wafers to a million possible defects. Then we use SIM vision to sample a thousand of those possible defects, which trains our Extract AI software, then Extract AI uses inference to classify all of the other potential defects on the wafer. That's the synergy we've created between optical, eBeam and AI.



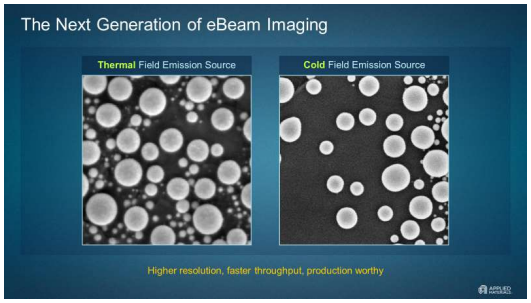

Second is PROVision. PROVision shares the eBeam imaging quality of SEMVision but is optimized for speed. When we first introduced PROVision in 2016, it was mainly used for eBeam inspection. However, eBeam inspection is a relatively small market. As Maayan described, technology inflections are creating new and larger opportunities for PROVision, which we call emerging SEM metrology. These include eBeam overlay at ADI and AEI process steps and massive metrology, which generates big inline data, both across the wafer and through multiple layers.




Third, our VeritySEM is our CDSEM product used to precisely measure critical dimension uniformity. As I mentioned during the introduction, Applied is second in overall process control revenue, but we are number one in eBeam revenue, and we are significantly outgrowing the process control market this year, thanks to our eBeam leadership, technology inflections that need our eBeam technology and the unique ways we're combining eBeam with our other technologies to give customers new ways to accelerate “t.” Recently, Gary alluded to new technology in our PDC group that we're introducing to our customers. Today I'm happy to share a little more information with you.




The technology is called “cold field emission” or CFE. It has two simultaneous benefits. First, it enables sub-nanometer resolution. Second, we can produce two to five times more electrons at the same resolution as conventional eBeam technologies.



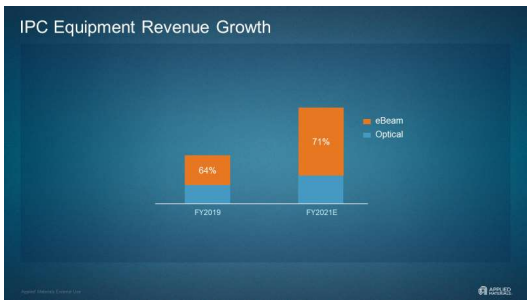

This means we can give process engineers yield critical information that they've never been able to see until now -- even faster. We're already sampling eBeam products with CFE technology to our customers, and the response is very positive and strong. Now I'd like to show you that the way our customers use our products can differ from the way third party researchers categorize them.


Specifically our Enlight optical wafer inspection systems simultaneously uses brightfield and darkfield technologies to identify potential defects. But in this third-party report, the revenue is only reflected in the darkfield category. More importantly, all PROVision revenue is categorized as eBeam inspection, but as we showed you today, PROVision is primarily used for metrology. We don't envy the challenge researchers have adapting to the technology inflections and the new ways customers are deploying technologies. We'll work with them to potentially update some of the categories. In the meantime, we're mainly interested in helping you navigate the differences and avoid potential confusion.

Finally, I'd like to talk about our growth objectives and show you some of the progress we're making. In the investor meeting in April, we shared our 2024 target financial model. In our base case, we plan to grow our semiconductor systems revenue at about 1.5 times the rate of the WFE market. And we expect to increase Semiconductor Systems operating margins. IPC has an important responsibility to help enable this performance. As we discussed today, our strategies are designed to help drive growth in other businesses, including CVD, etch and services grow faster than the process control market and deliver attractive operating margins.


In April we also showed you the growth of our IPC business in three, four year periods, 2013 through ‘16, 2017 through ‘20, and our targets for 2021 through ‘24. As you can see from the chart, we grew IPC revenue by 40 percent from the first period to the second. And our goal is to grow more than double this rate from the second period to the third.

We believe we're on track to do this based on the technology inflections in our markets, the breadth and strength of our portfolio and the unique ability we have to help enable PPACt for our customers. As we said on our most recent earnings call, we plan to increase our PDC system revenue by over 60 percent this calendar year.




What's driving this outperformance is the eBeam technology inflections we discuss today. This slide shows IPC group revenue in fiscal 2019, and our expectations for revenue in 2021. You can see how eBeam is growing to become around 70 percent of the IPC revenue this year. A centerpiece of our growth is PROVision and the emerging SEM metrology applications we talked about today.


Here is our current expectations for PROVision revenue this fiscal year, as compared to 2019 and 2020. You can see that we expect to increase PROVision revenue by over 80 percent, achieving revenue of around $200 million. That's above the 60 percent growth we achieved in fiscal 2020.

And now Maayan, Lior and I would be happy to take your questions about today's Master Class.

Mike, let's begin the Q and A.