APPLIED MATERIALS®

2023 SEMICON West Technology Breakfast

Forward-Looking Statements and Other Information

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, the path to net zero and our environmental goals, our investment and growth strategies, our development of new products and technologies, the EPIC Center, our business outlook, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; global economic, political and industry conditions, including rising inflation and interest rates; the implementation and interpretation of new export regulations and license requirements, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies; our ability to obtain licenses or authorizations on a timely basis, if at all; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; failure to realize the anticipated benefits of our planned investments; construction delays, cost increases or changes in investment or construction plans related to the EPIC Center; the effects of regional or global health epidemics, including COVID-19; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; our ability to achieve environmental, social and governance strategies, commitments and targets; and other risks and uncertainties described in our filings with the U.S. Securities Exchange Commission, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

Welcome

Mike Sullivan

Corporate Vice President

Investor Relations

AGENDA

7:30 Mike Sullivan
Welcome

7:35 Dr. Prabu Raja
EPIC™ Opportunities

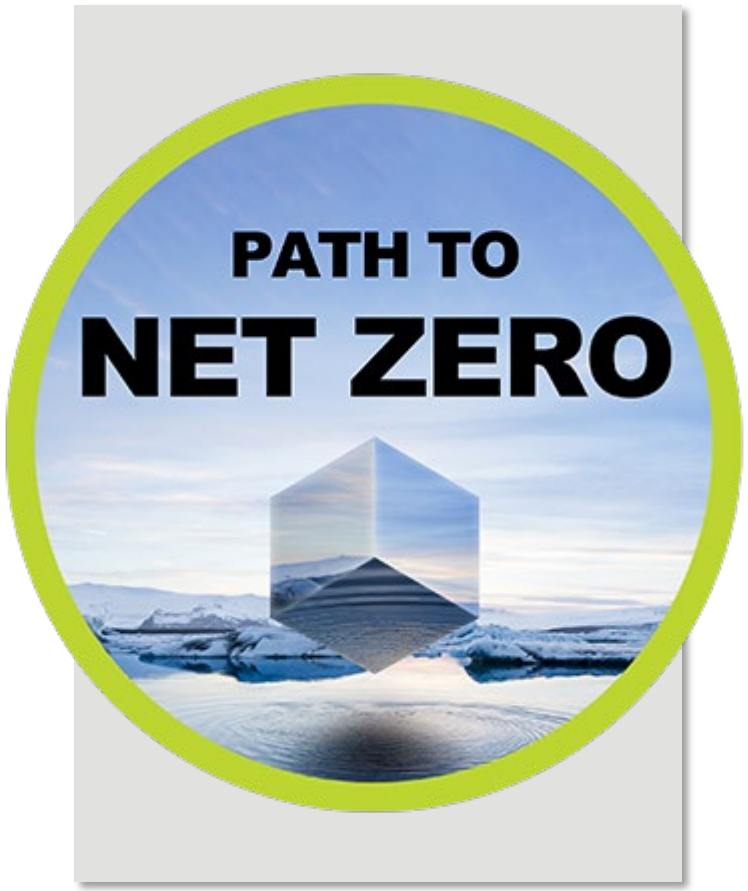
7:50 Mike Rice
Vistara™ and EcoTwin™

8:05 Dr. Sundar Ramamurthy
Heterogenous Integration (HI)

8:15 Vincent DiCaprio
HI Panel

9:00 Adjourn
Q&A Mingle

SEMICON West 2023 Themes



$1T Industry Growth Challenges

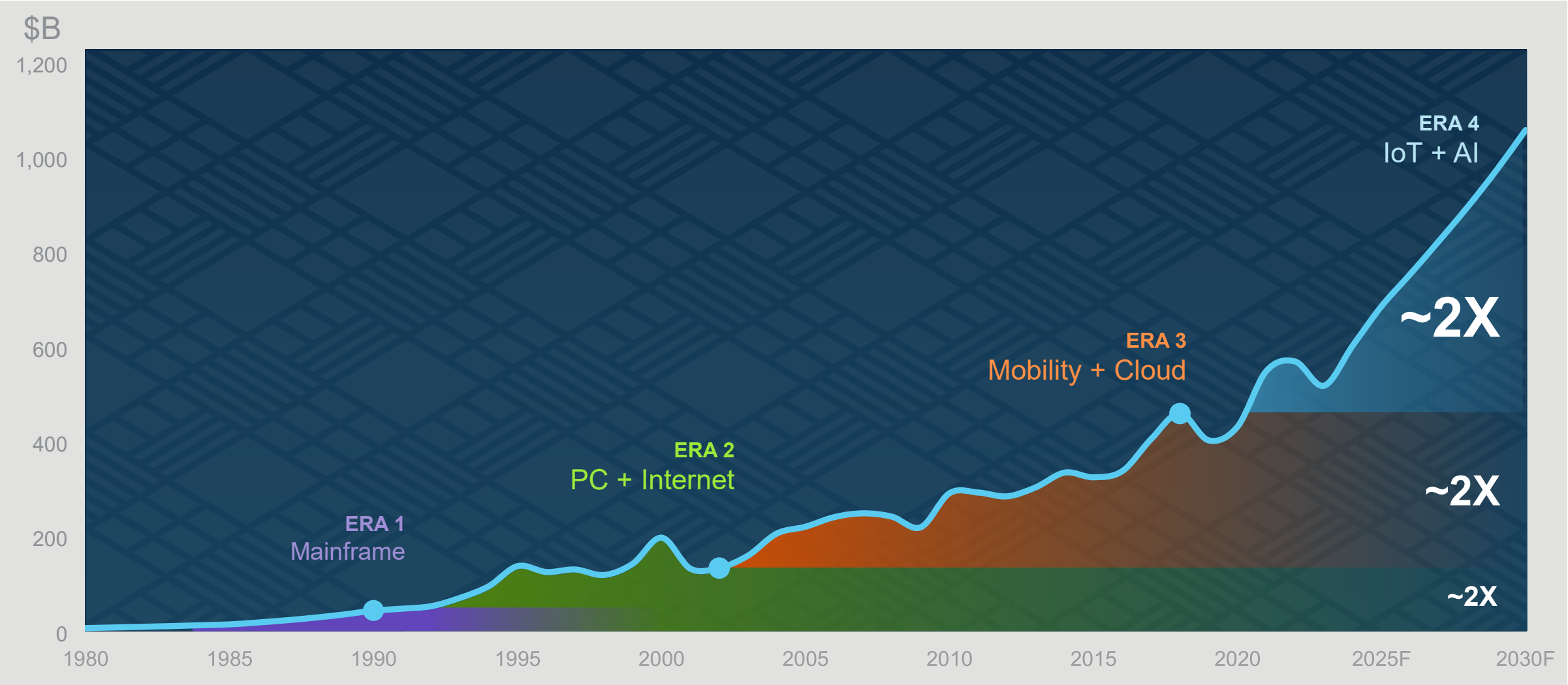
Epic Opportunities

Dr. Prabu Raja

President

Semiconductor Products Group

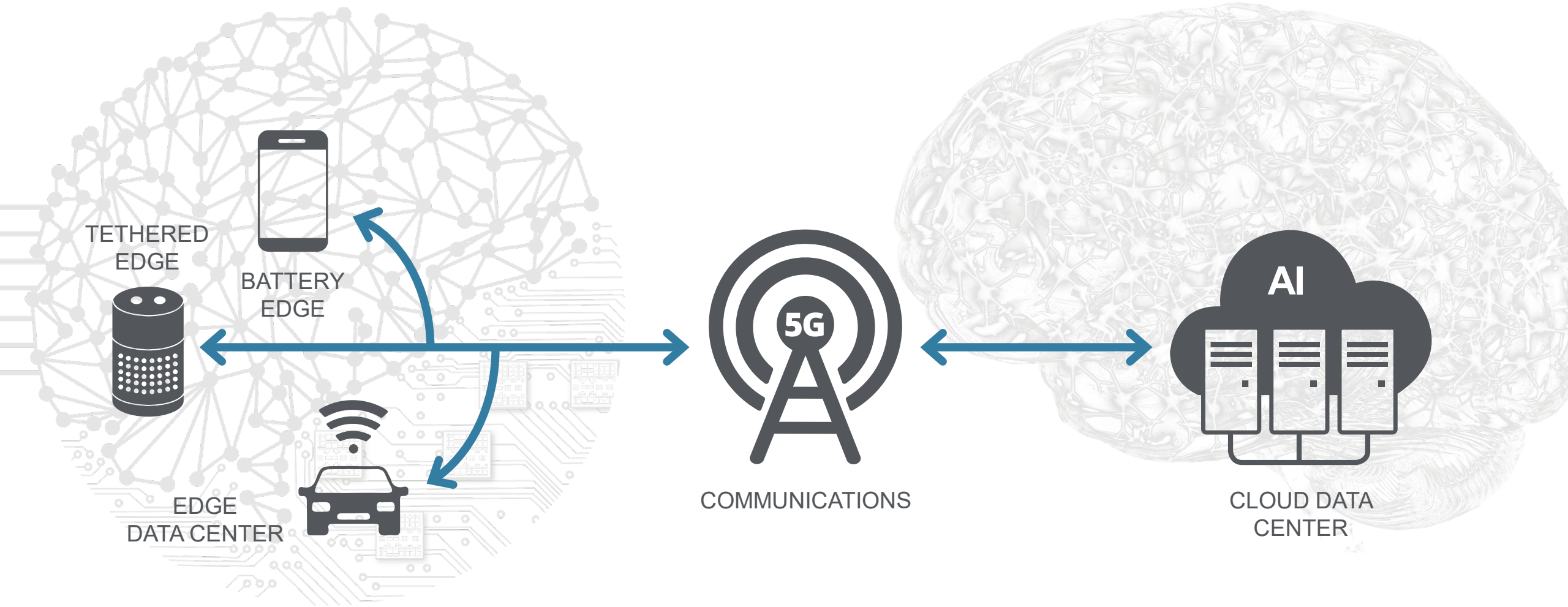
Path to a $1T Semiconductor Industry



Source: SIA, Applied Materials - SMI

Each computing era ~doubles size of semiconductor market

Internet of Things and Artificial Intelligence Era



ICAPS NODES

LEADING EDGE

Clean Energy Revolution Needs ICAPS and Leading-Edge Silicon

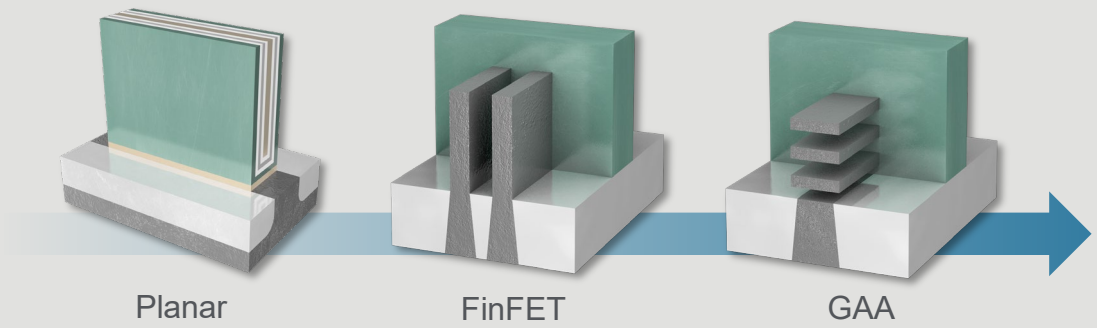
Electric Vehicles

Wind and Solar

Smart Grid

Significant Challenges Across the Semiconductor Industry

Complexity

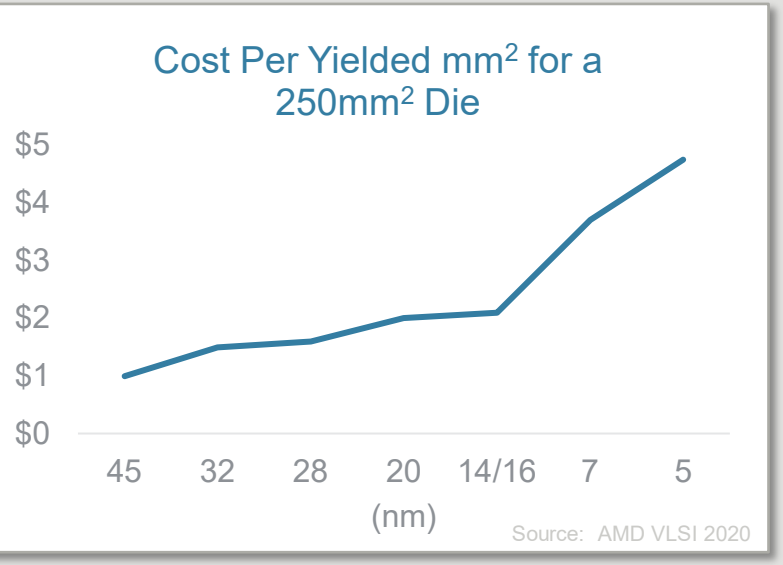


College Grads

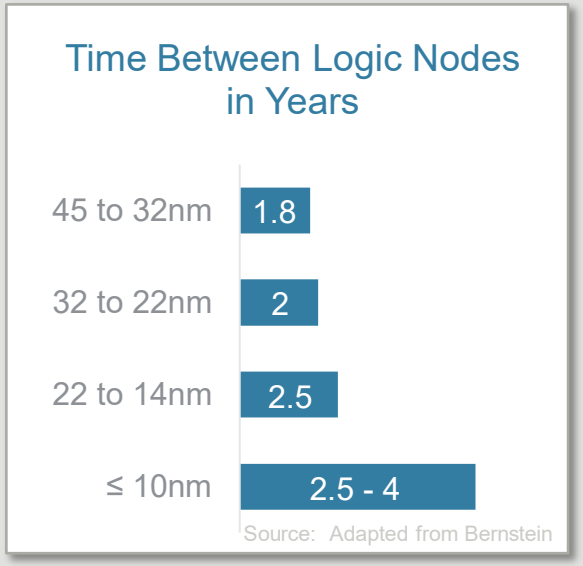
- 1,000,000: additional skilled workers needed by 2030
- 100,000: number of graduate students enrolled in electrical engineering and computer science in the U.S. annually

Source: Deloitte

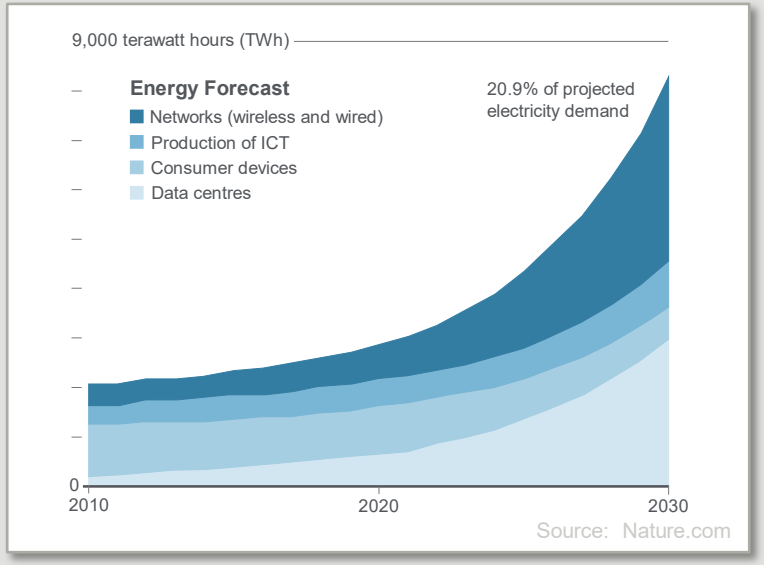
Cost



Cadence

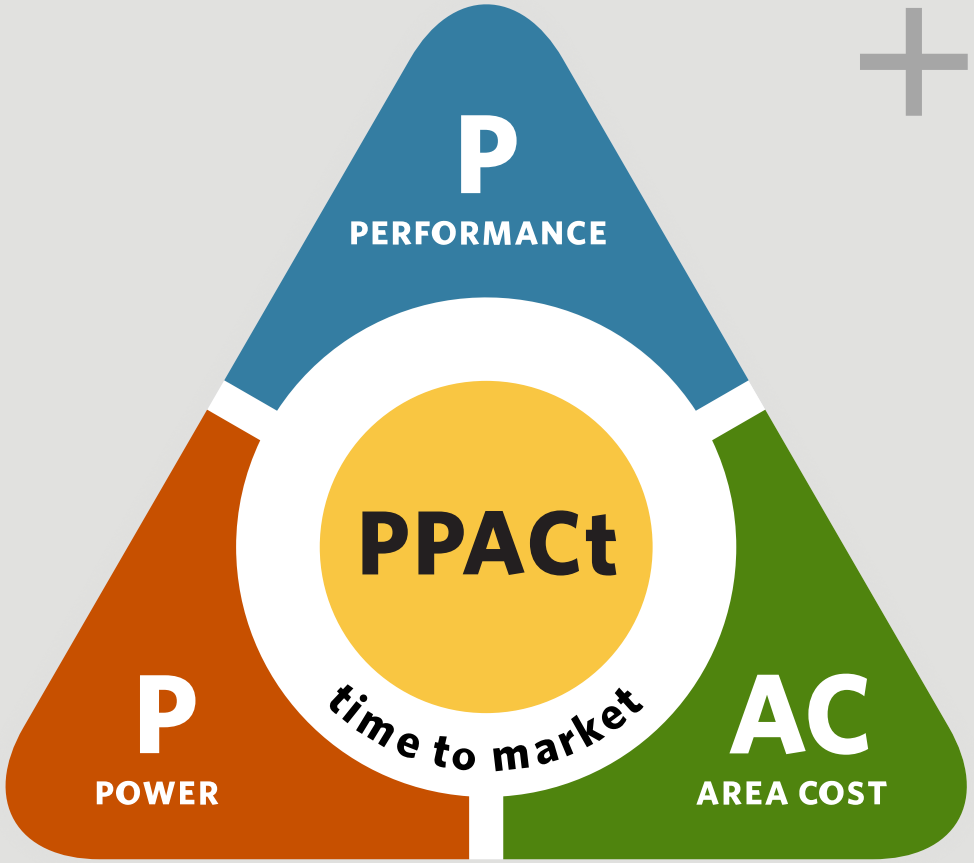


Carbon Emissions



APPLIED MATERIALS

New Playbook for Innovation and Commercialization



+ EPIC™ CENTER

PPACt™ solutions

- New materials
- 3D structures
- Atomic-level precision
- Connected capabilities
- System-level innovations

New collaboration models

- Across industry and academia
- Growing global talent pool

Net Zero

- Energy efficient semiconductors and manufacturing operations

Key Playbook Elements

Inclusive innovation to accelerate commercialization

- Equipment and processes → device validation - *EPIC™ Center*
- Engineering of technologies → products - *Collaborative Engineering Center, India*
- Foundational research & talent development - University Innovation Networks, *ASU*

New products for integrated processes

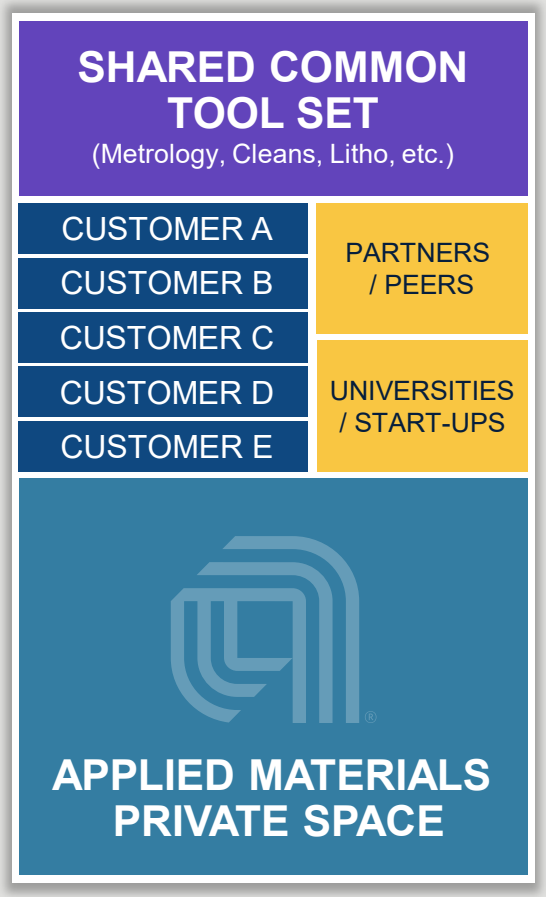
- Flexible, intelligent and sustainable products with greater integration capabilities - *Vistara™*
- Integrated Materials Solution®
- AI^{x} Actionable Insight Accelerator™
- EcoTwin™

System-level innovations for PPACt™ acceleration

- System Technology Co-optimization (STCO) - *Heterogeneous Integration*

APPLIED MATERIALS

EPIC™ Center Implementation



*Conceptual layout only

FOR CHIPMAKERS AND INDUSTRY PARTNERS

Co-development and early validation to accelerate new devices and structures

- New materials
- New technologies
- New process flows

FOR UNIVERSITIES AND START-UPS

Co-development and early validations on new materials and technologies

- Accelerate commercialization of academic research
- Attract, inspire and train next-generation talent

Designed for high-velocity innovation and commercialization

New Commercialization Path

Idea

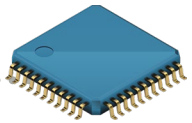
Proof of Concept

Commercial Equipment and Process

Technology Integrated into Module

Technology Integrated into Device

Commercial Chip



5 – 7 YEARS | 2 – 3 YEARS | 1 – 2 YEARS | 1 – 2 YEARS | 1 – 2 YEARS

Foundational Research → Equipment and Process Development → Module / Integration → Pilot → HVM

UNIVERSITY ENVIRONMENT | EQUIPMENT COMPANY | CHIPMAKER

Foundational Research

Equipment and Process Development

Module / Integration → Pilot → HVM

New collaborative lab models at partner universities

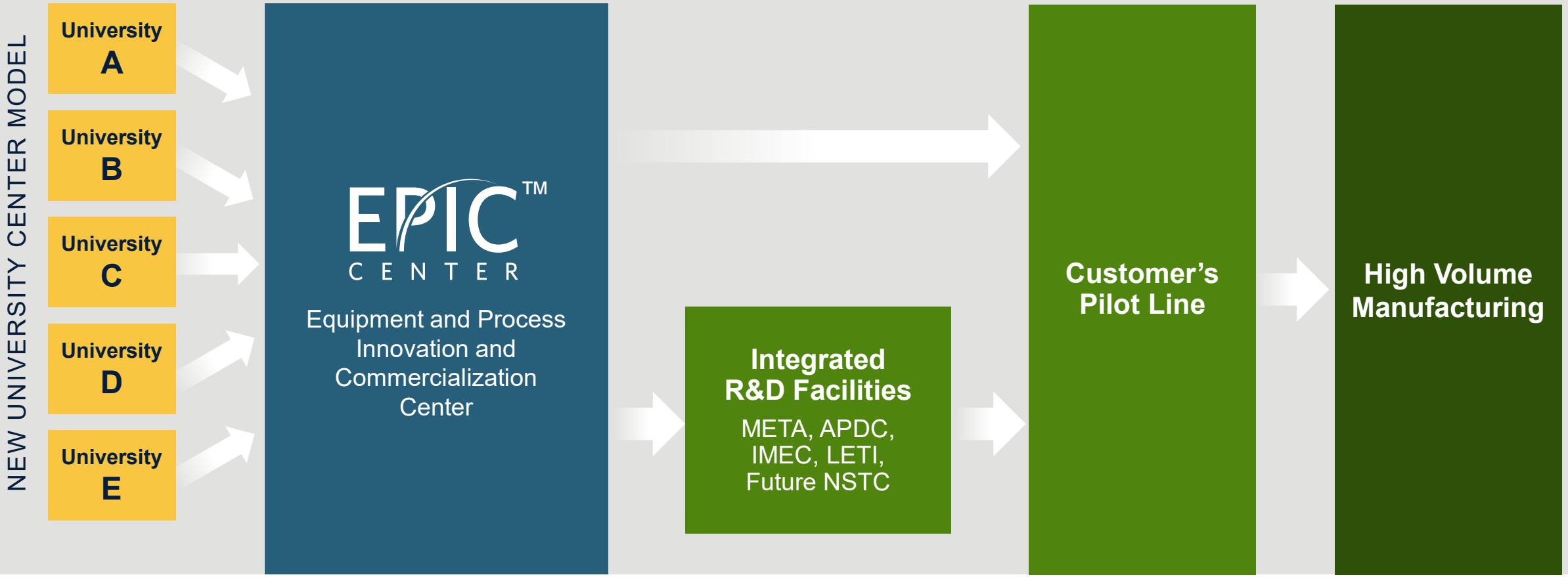
University / start-up access to EPIC™

Chipmakers' collaborative research within EPIC™ facility

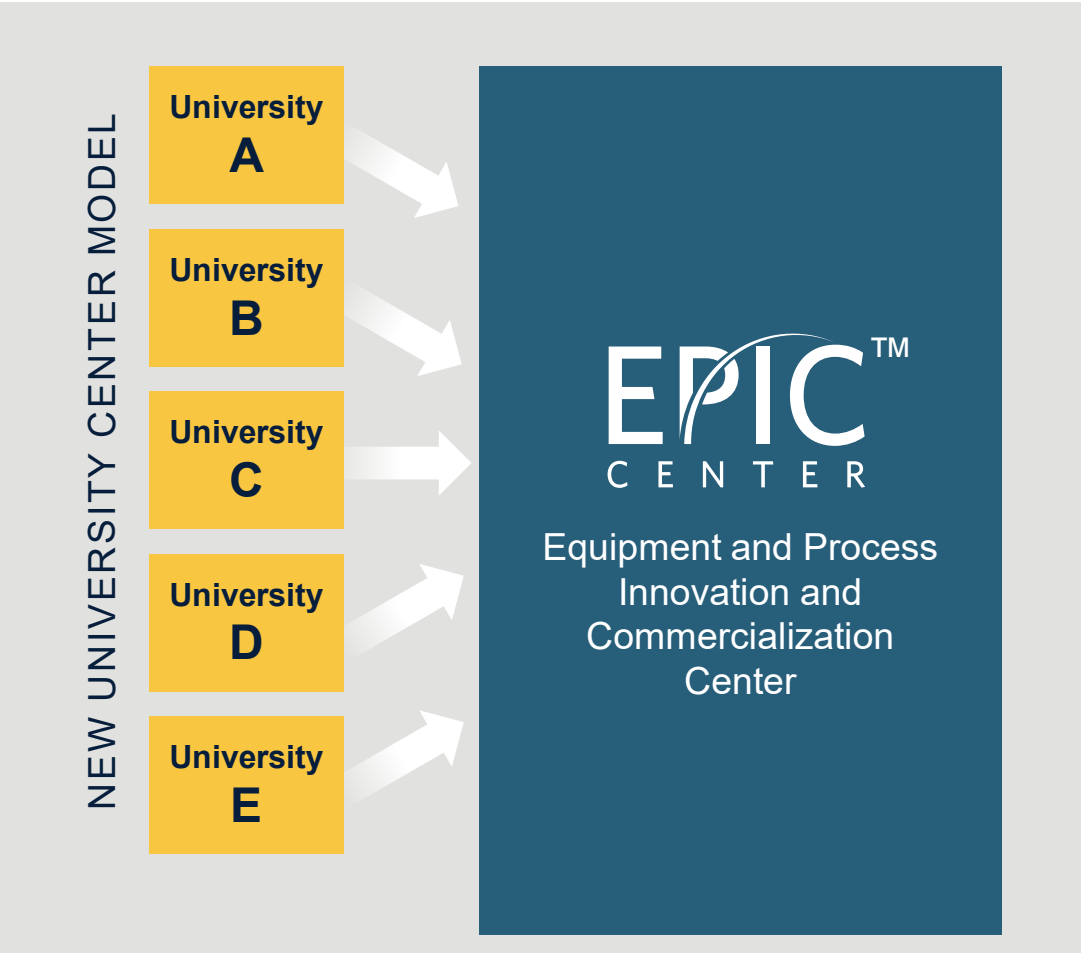
Work supported by full suite of Applied R&D capabilities

2 - 4 year acceleration

New EPIC™ Model



EPIC™ University Innovation Network



Foundational Research / C&F
(focused / thematic)

Innovation and Commercialization of Manufacturing Technologies
(unit processes + equipment + short loops)

New collaboration models to accelerate commercialization of innovations

- World-class shared R&D and prototyping facilities
- Access to industry partners, startups and government entities
- Talent development through hands-on learning and research

University Innovation Network: Materials-to-Fab Center

Press Release

ARIZONA STATE UNIVERSITY AND APPLIED MATERIALS TO CREATE 'MATERIALS-TO-FAB' CENTER AT ASU RESEARCH PARK

More than $270 million in corporate and state investment will help advance Arizona's semiconductor industry

TEMPE, Arizona and SANTA CLARA, Calif., – Arizona State University (ASU) and Applied Materials, Inc. today announced an alliance, aided by the Arizona Commerce Authority, that brings more

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System-level innovations for PPACt™ acceleration

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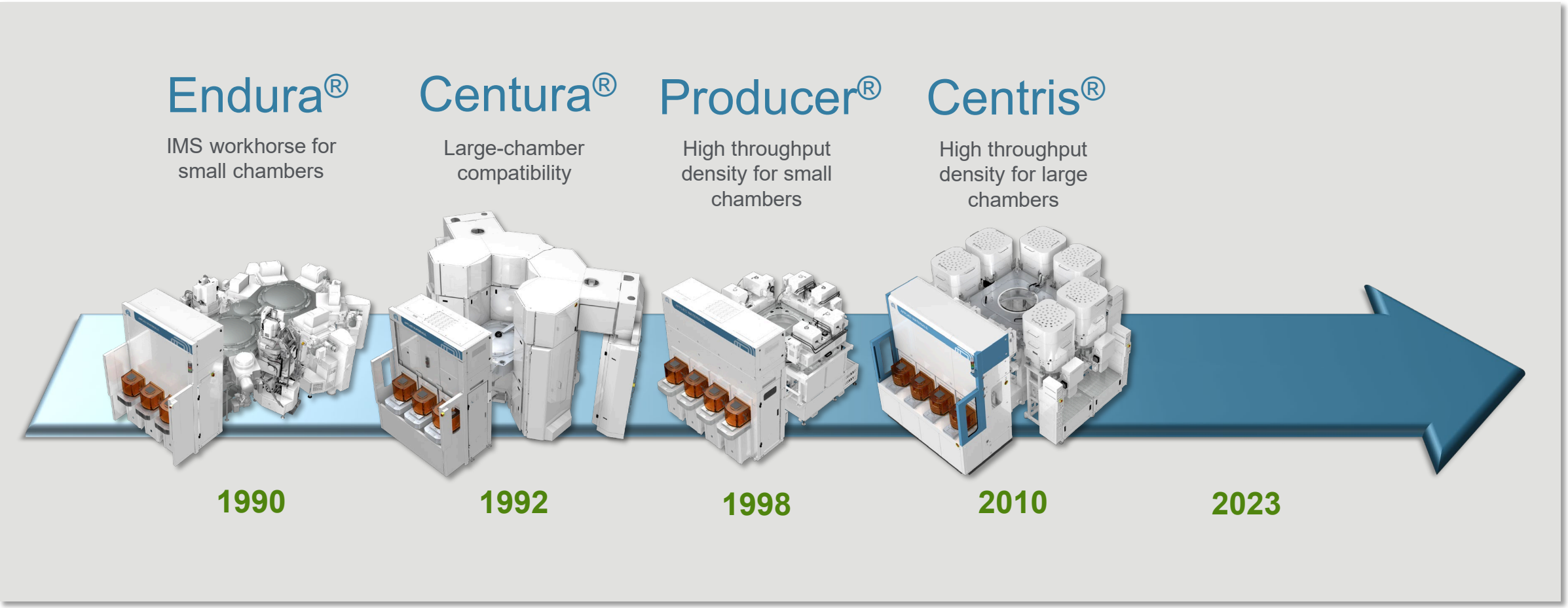
Introducing Vistara™

Mike Rice

Corporate Vice President, Semiconductor Products Group

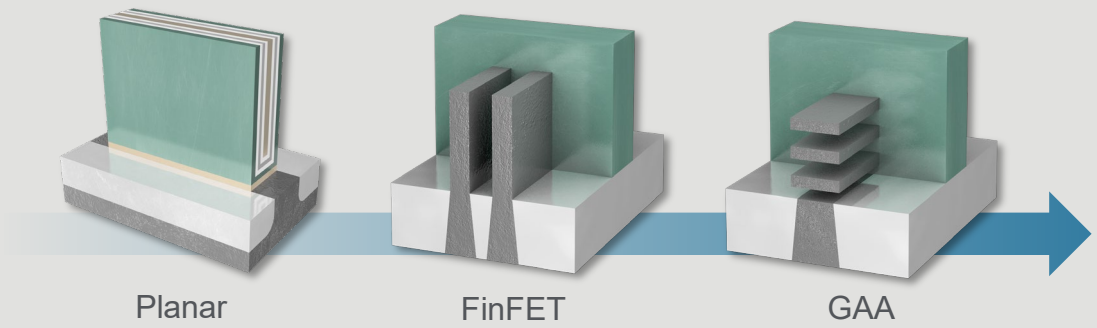
Applied Materials Fellow

A Long History of Successful Platforms



Significant Challenges Across the Semiconductor Industry

Complexity



College Grads

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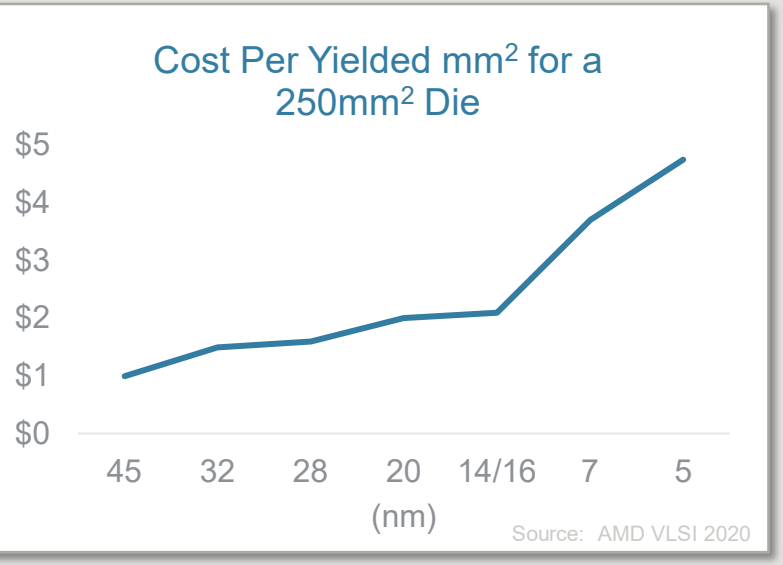
Source: Deloitte

Cost



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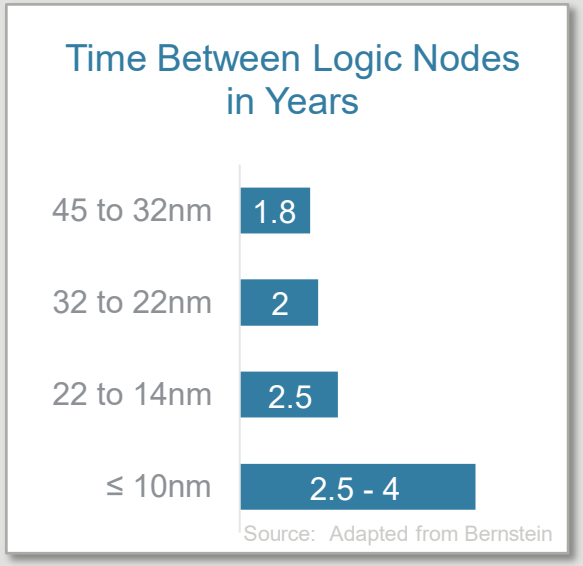
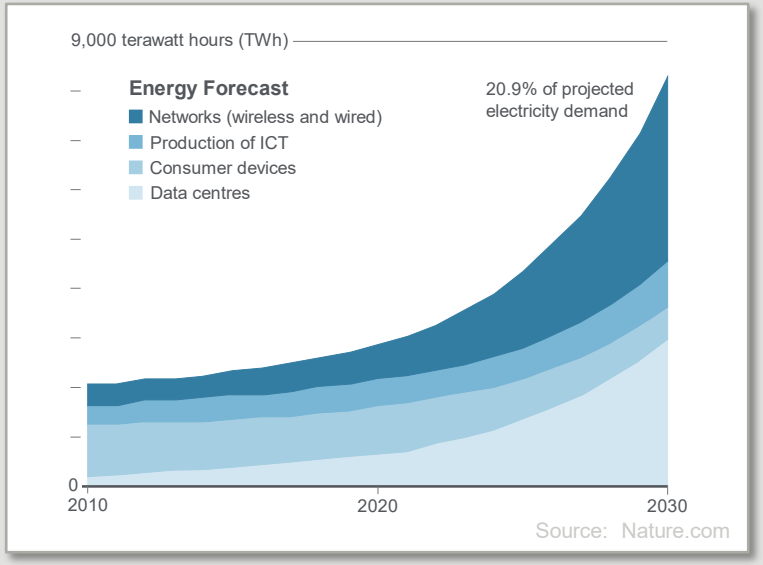
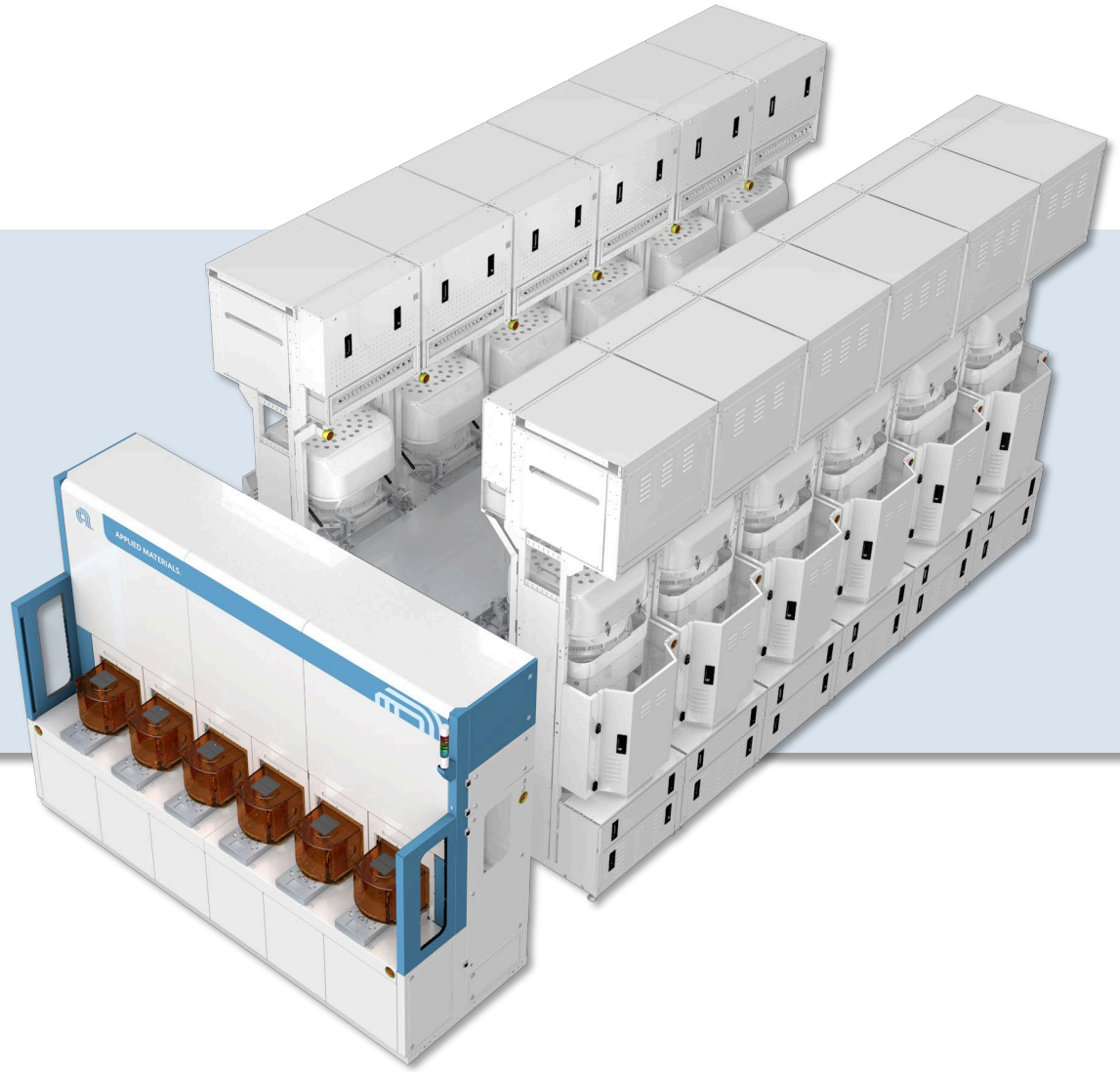


Carbon Emissions



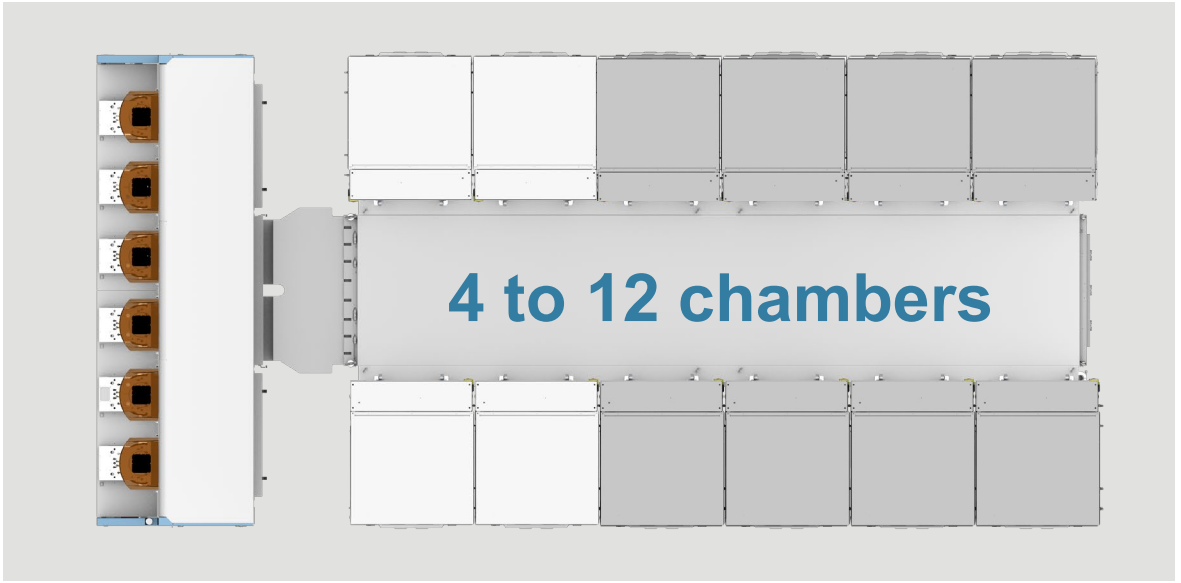
APPLIED MATERIALS

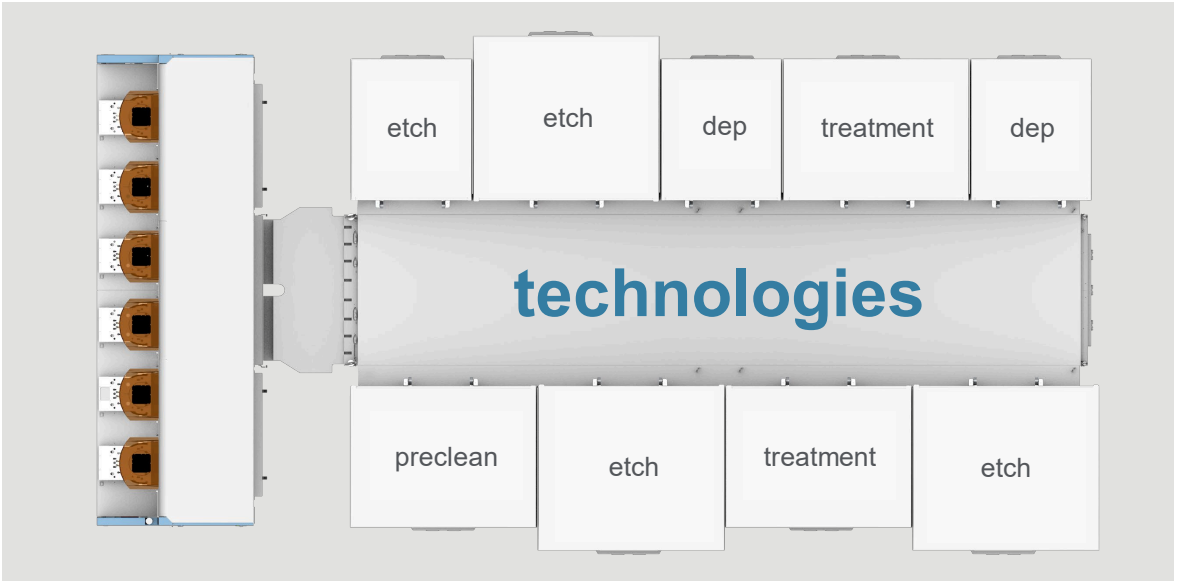
Introducing the Applied Vistara™ Platform

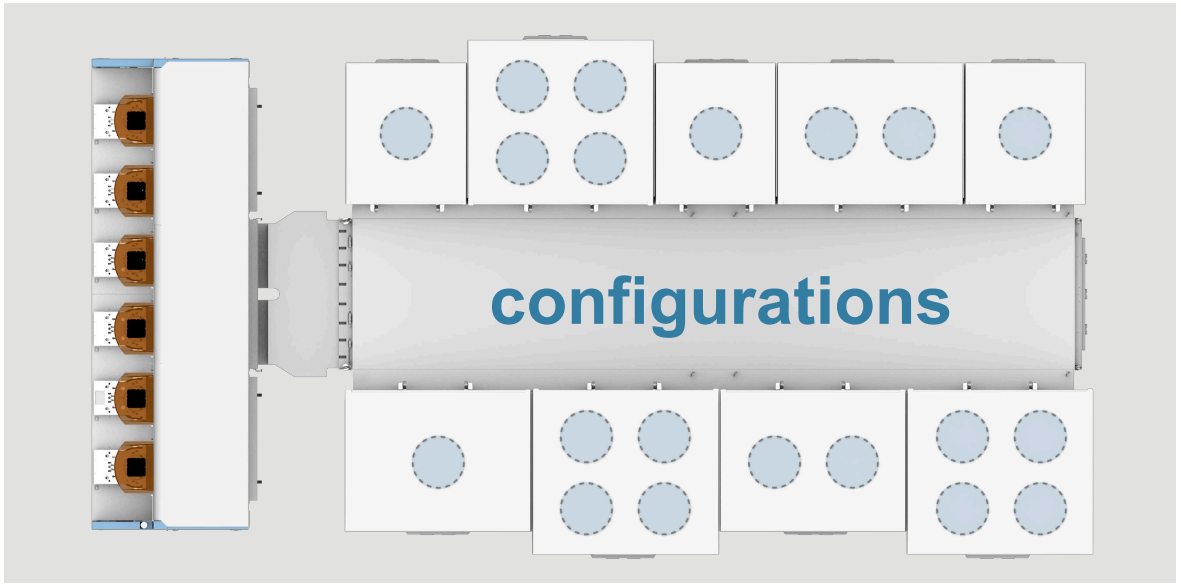


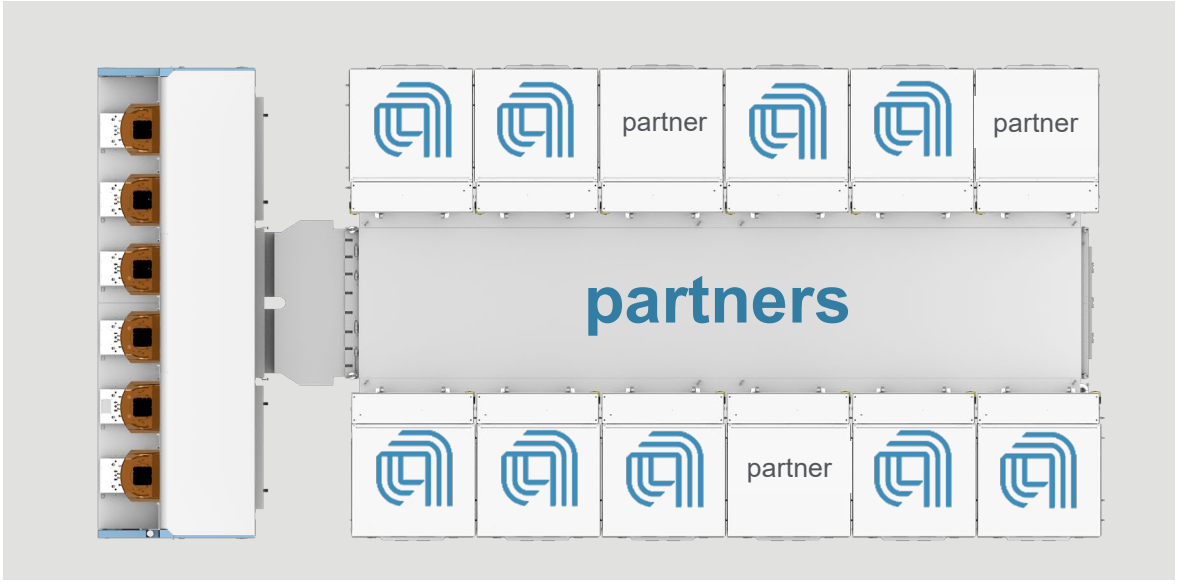
- ✓Flexibility
- ✓Intelligence
- ✓Sustainability

Vistara™ Platform Chamber Flexibility





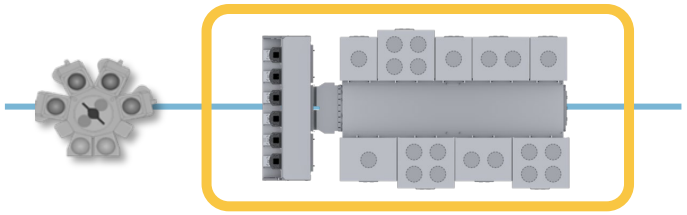




A Flexible Platform for IMS™ Connected Capabilities

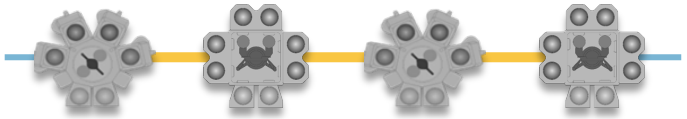
Increasing Process Integration

IMS™



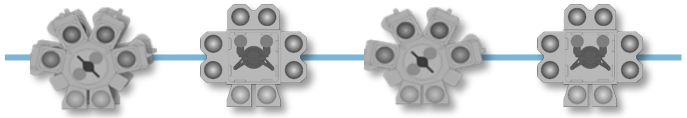
Multiple processes in one system, under vacuum

Co-optimized



Adjacent processes

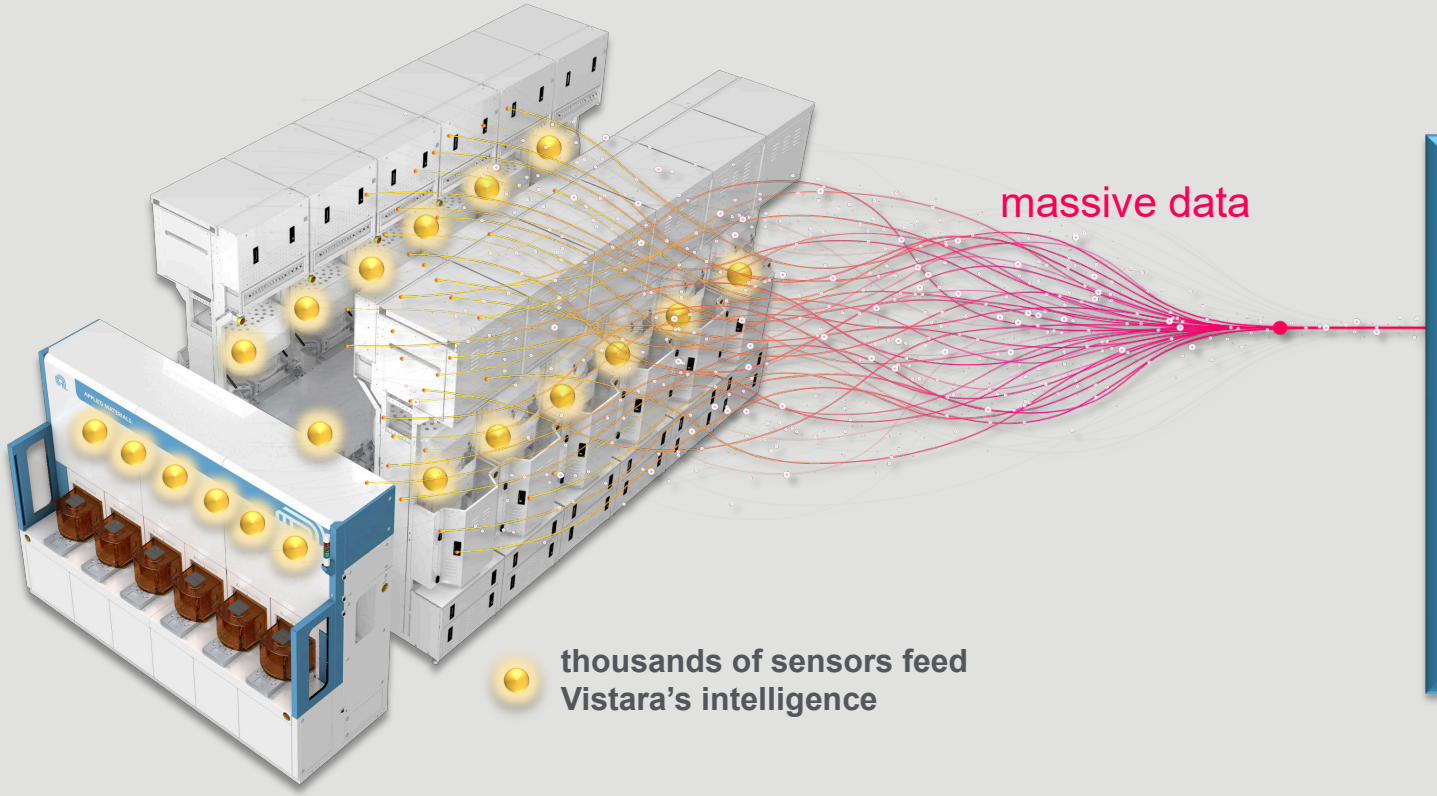
Unit Process



Single process

IMS™ = Integrated Materials Solution®

Vistara™ Platform Intelligence



massive data

thousands of sensors feed Vistara's intelligence

AIX™

- Accelerate R&D
- Speed transfer and matching
- Maximize output and yield

EcoTwin™

- Intelligence for sustainability

Accelerating time to market and maximizing ROI and sustainability across the entire lifecycle

Make Possible a Better Future

ecoUP™

Sustainability Initiative

3x30 Goal

↓30% Equivalent Energy

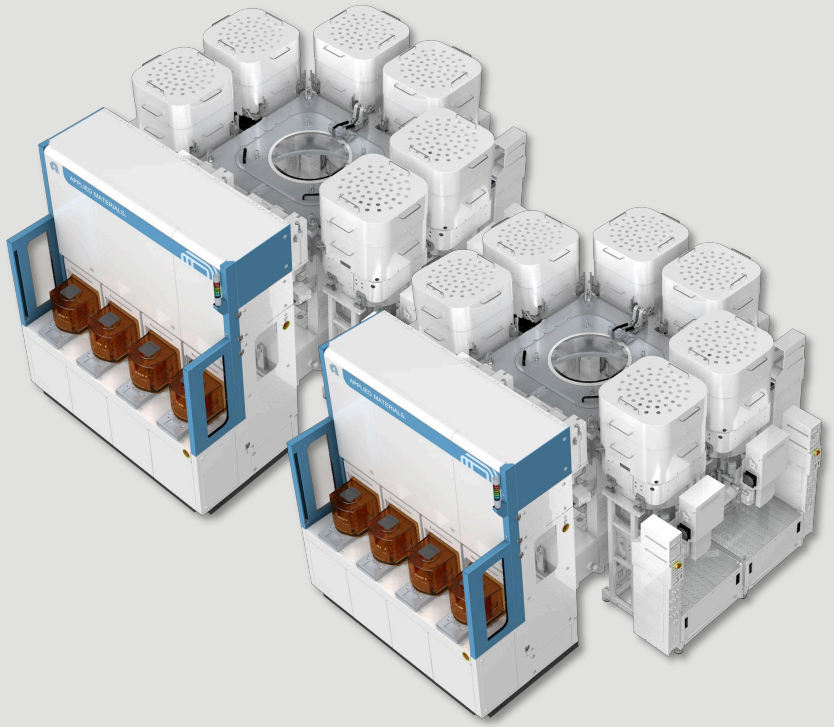
↓30% Chemical Consumption

↓30% Cleanroom Area per Wafer

by 2030

Vistara™ Platform Energy Savings

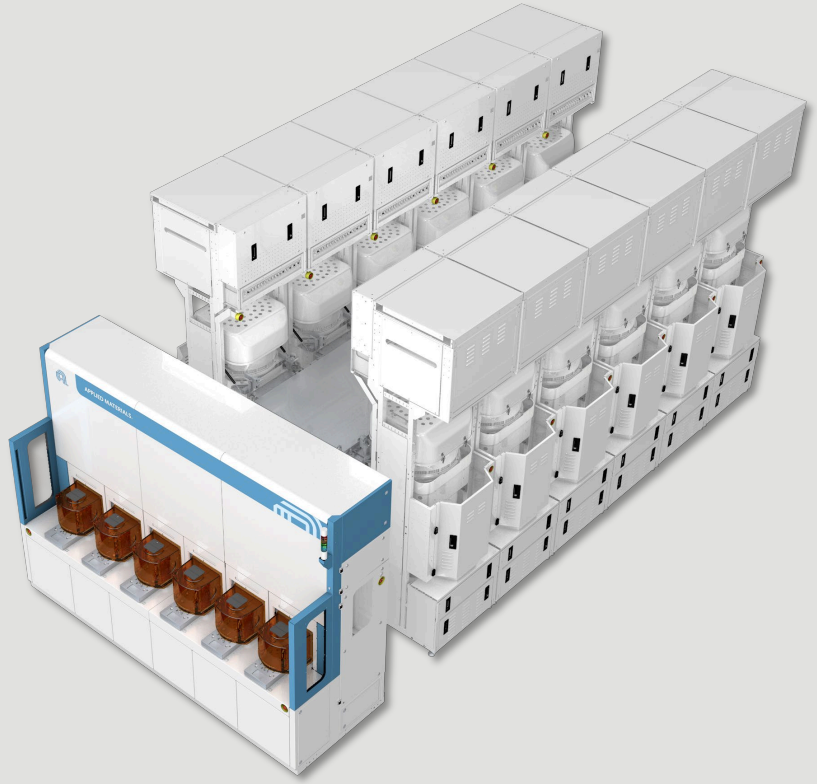
Centris® Platform
12 chambers



~35% platform energy savings

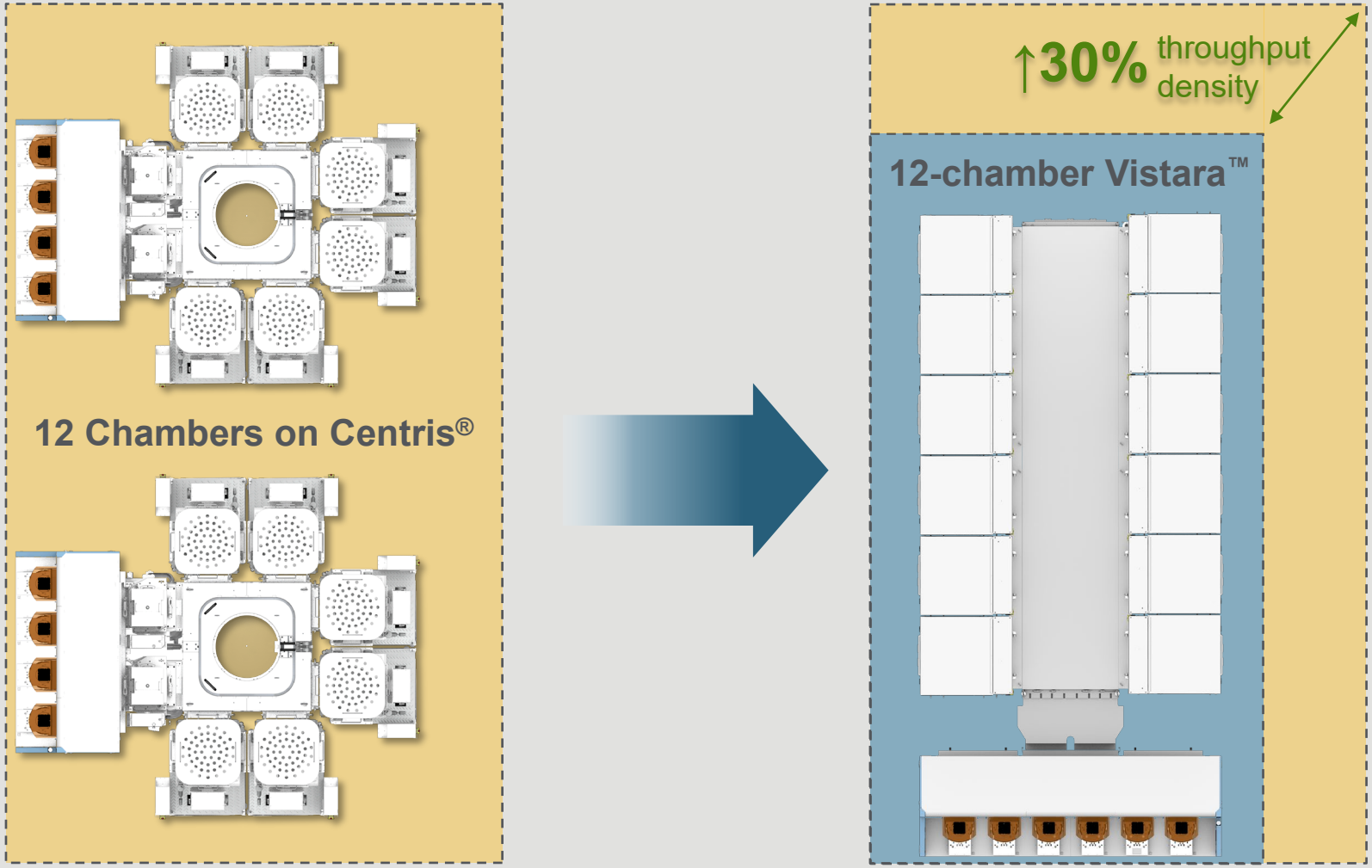
~10% system* energy savings

Vistara™ Platform
12 chambers

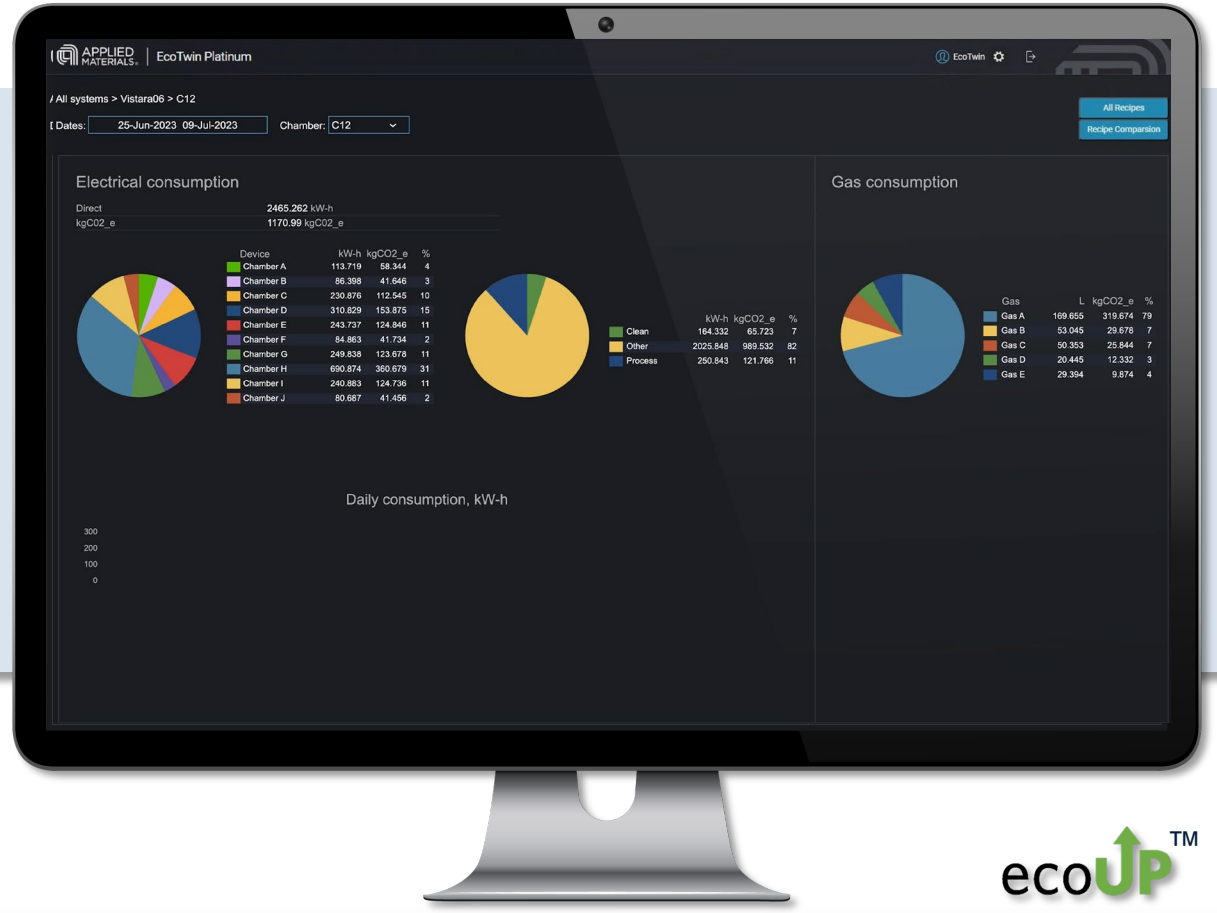


* Systems configured for Sym3 Etch chambers

Vistara™ Footprint Savings



Introducing EcoTwin™ Eco-Efficiency Software



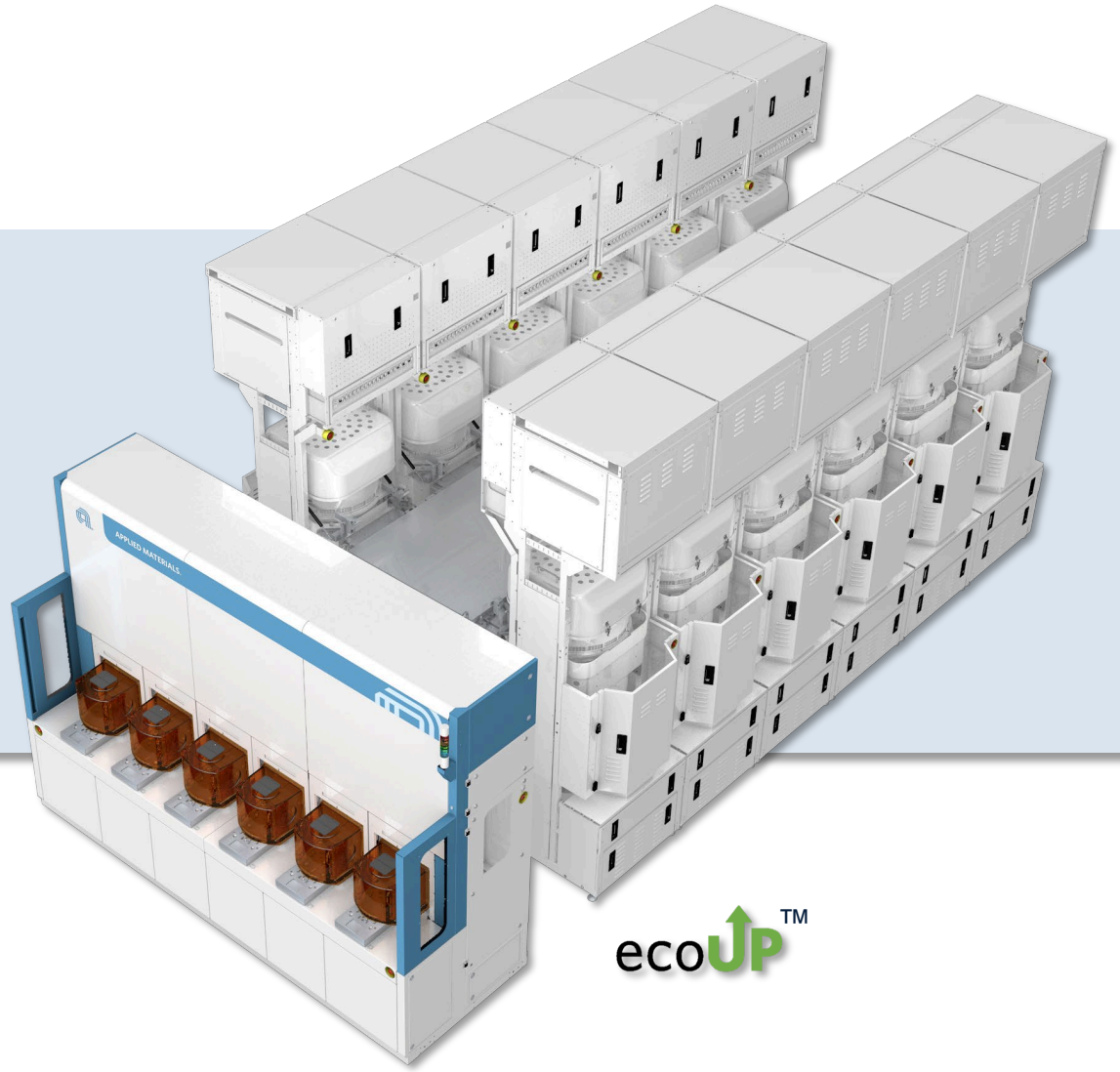
- ✓ **Compare** resource consumption of different recipes to optimize sustainability
- ✓ **Monitor** energy and gases in real-time to assess environmental impact of chambers, platform and sub-fab components
- ✓ **Report** continuous improvements in environmental performance

ecoUP™

Demonstrated >30% reduction in CO_2/wafer in a memory etch application

APPLIED MATERIALS

The most flexible IMS-ready platform!



ecoUP™

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- ✓Intelligence
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System-level innovations for PPACt™ acceleration

- System Technology Co-optimization (STCO) - *Heterogeneous Integration*

Heterogenous Integration

Dr. Sundar Ramamurthy

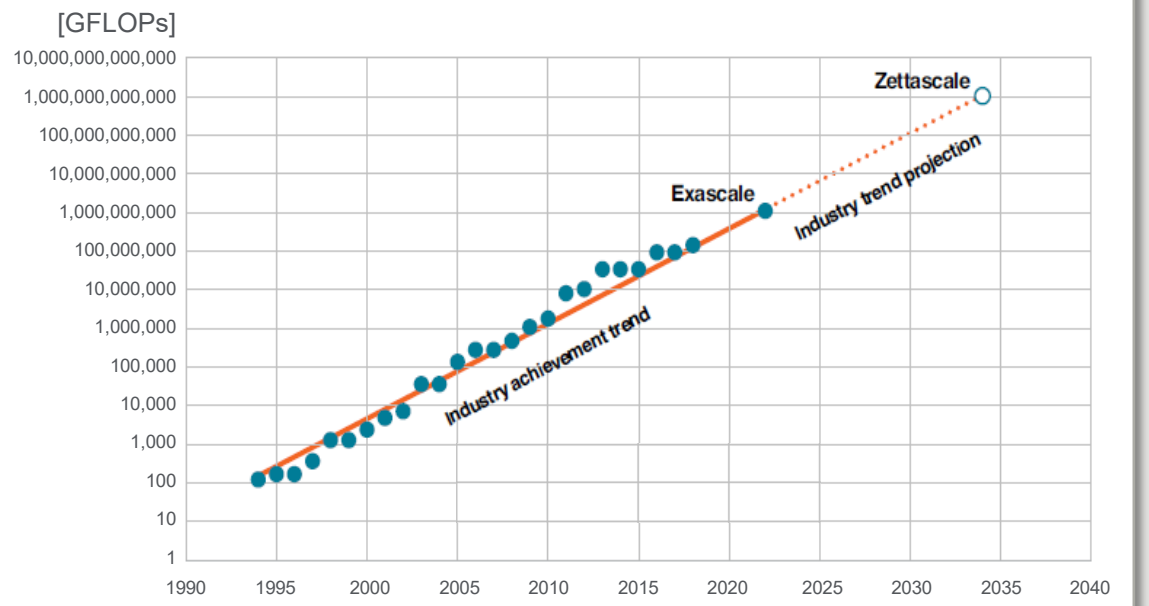
Group Vice President

Heterogenous Integration, ICAPS and Epitaxy

Semiconductor Products Group

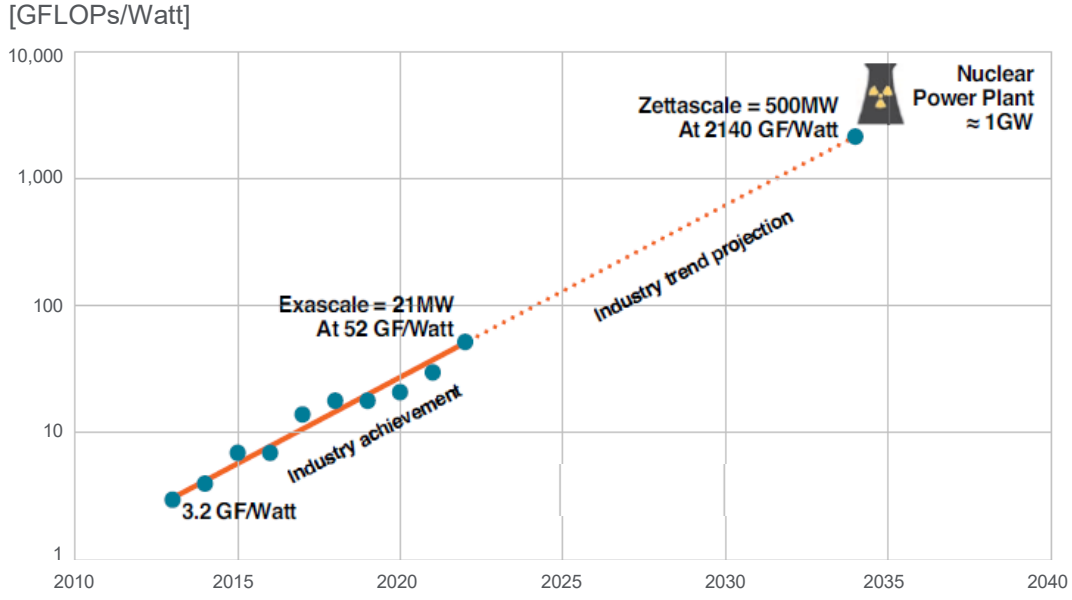
Performance Outpacing Power Efficiency

Performance Grows 2x every 1.2 Years



Source: L. Su, ISSCC 2023

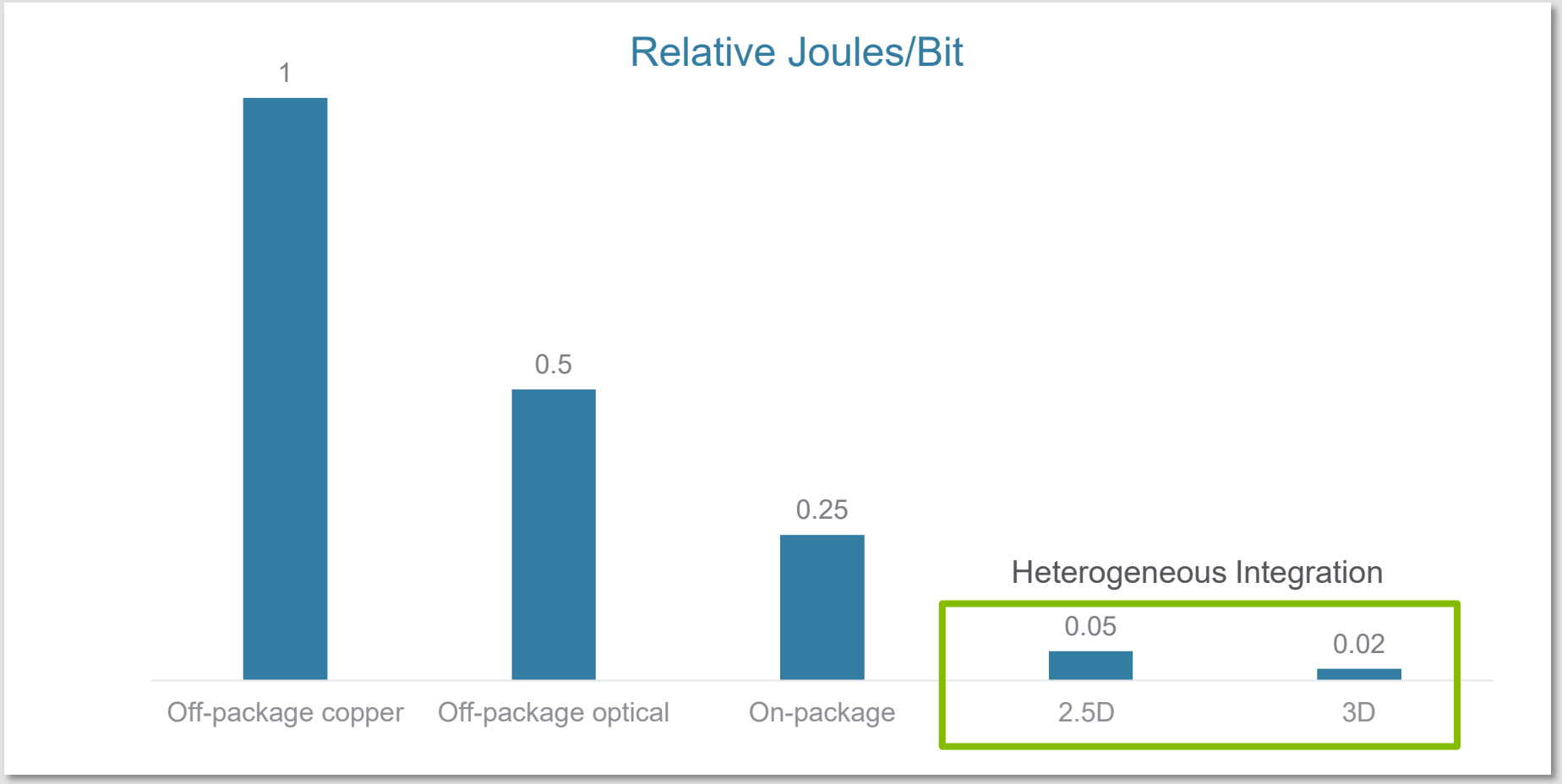
Power Efficiency Grows 2x every 2.2 Years



Source: L. Su, ISSCC 2023

Key Design Goals: ↑ Bandwidth ↓ Latency ↓ Power

Heterogeneous Integration Reduces Power



Source: Adapted from L. Su, ISSCC 2023

Heterogeneous Integration Improves PPACt™

Power

Performance

Shorter, parallel interconnects

Higher bandwidth

Lower latency

Lower power

50x lower power

Hybrid bonding vs. PCB chip-to-chip connection

Source: Adapted from L. Su, ISSCC 2023

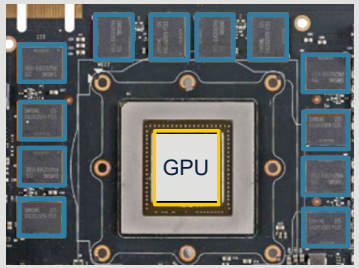
3D stacking

Tighter integration

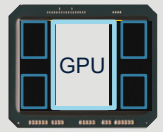
Many more chips per package

Higher bandwidth

GDDR5



HBM



~3X system performance

~50% lower power

Source: Samsung whitepaper

Compared to disaggregated dies on a PCB

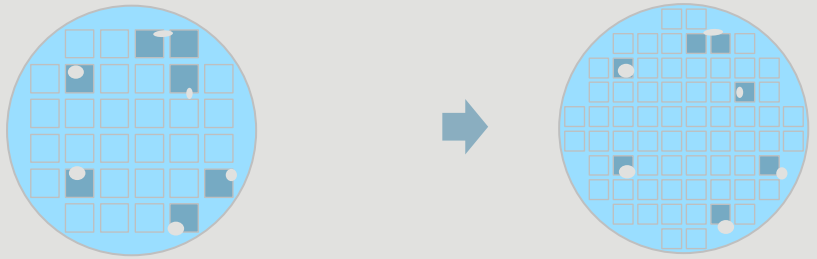
Area **C**ost

time-to-market

Chiplets

Higher yield

Reuse IP blocks



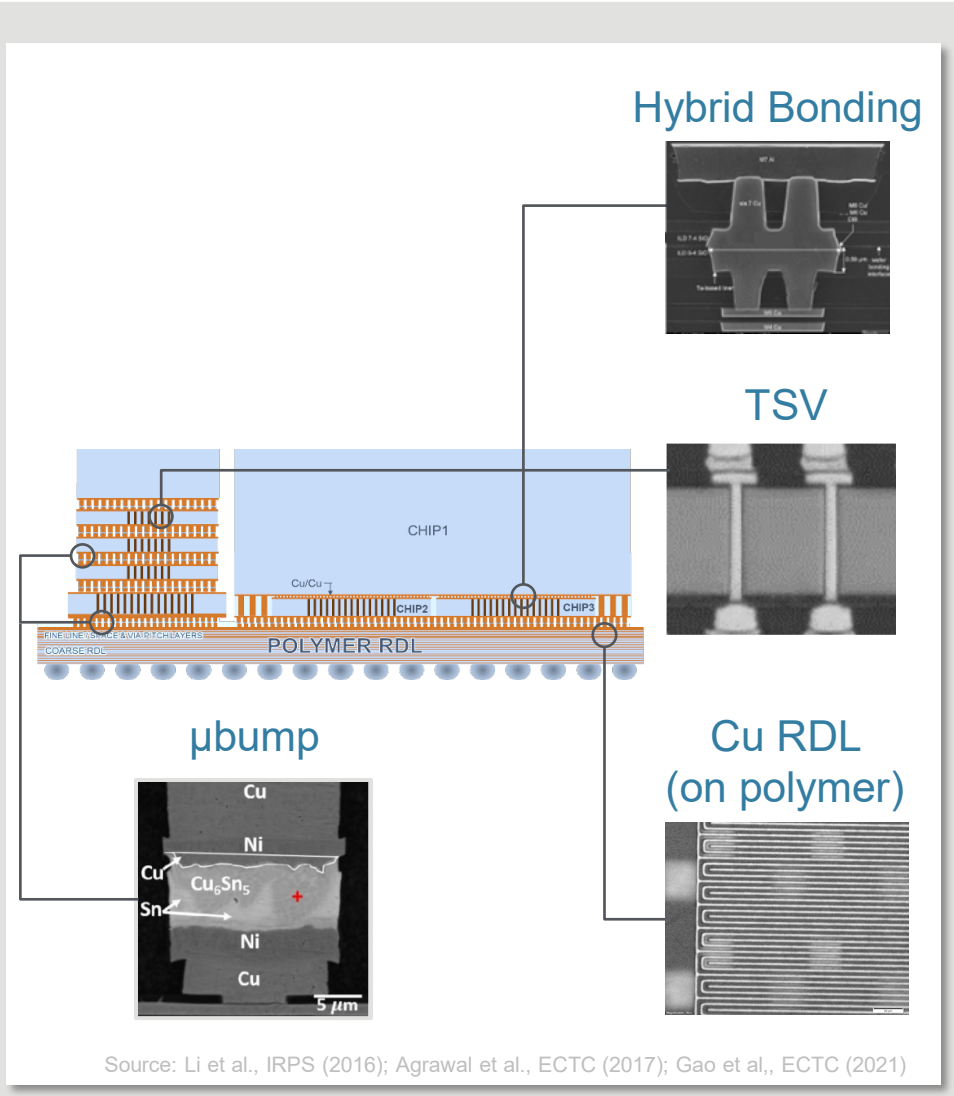
~60% lower cost

vs. 900mm chip partitioned into 3 die and 3D stacked

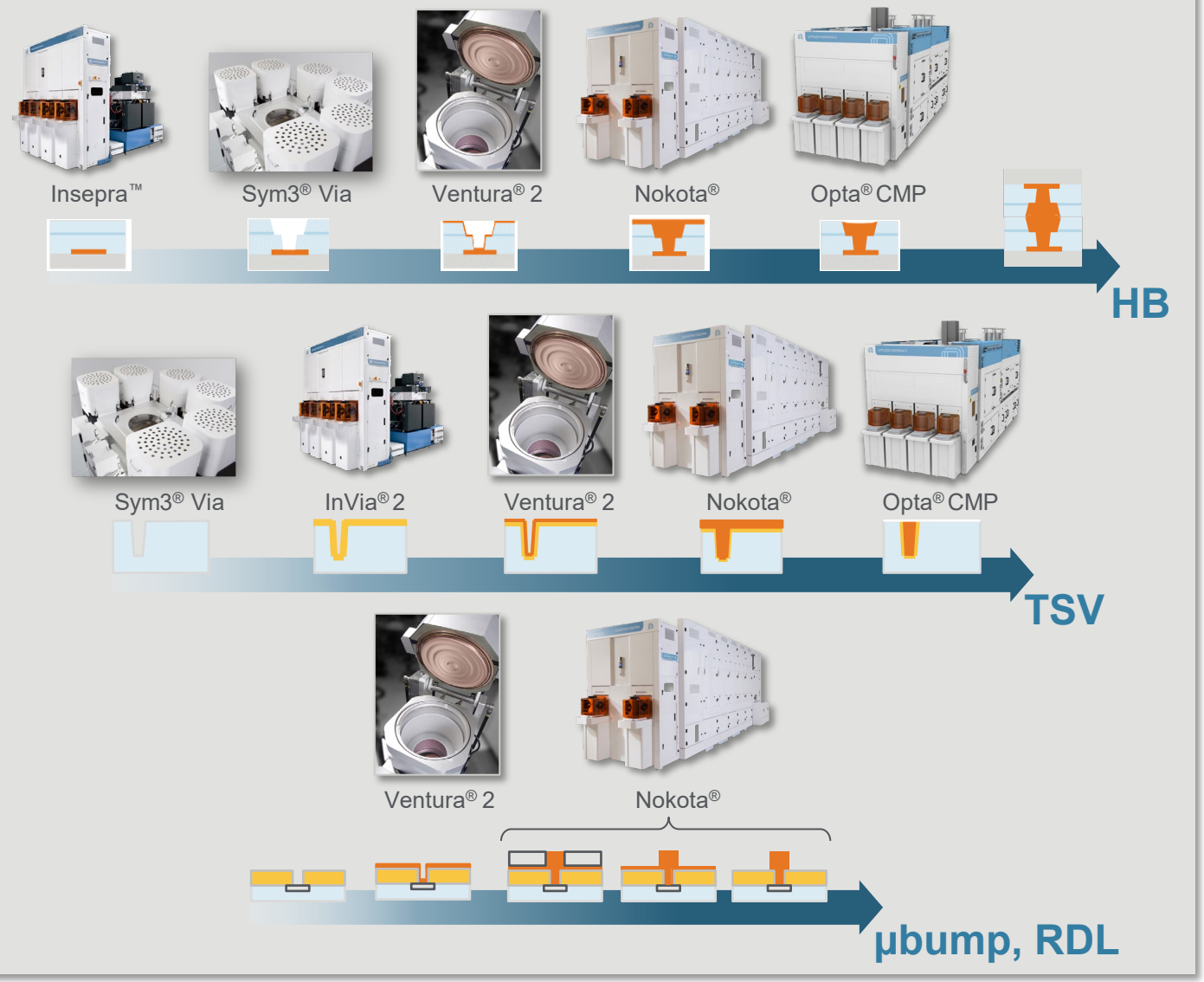
Source: A. Steengen, IMEC (Semicon Korea 2018)

Compared to large and specialized SOC chips

System-Level Integration with 2D and 3D Heterogeneous Integration

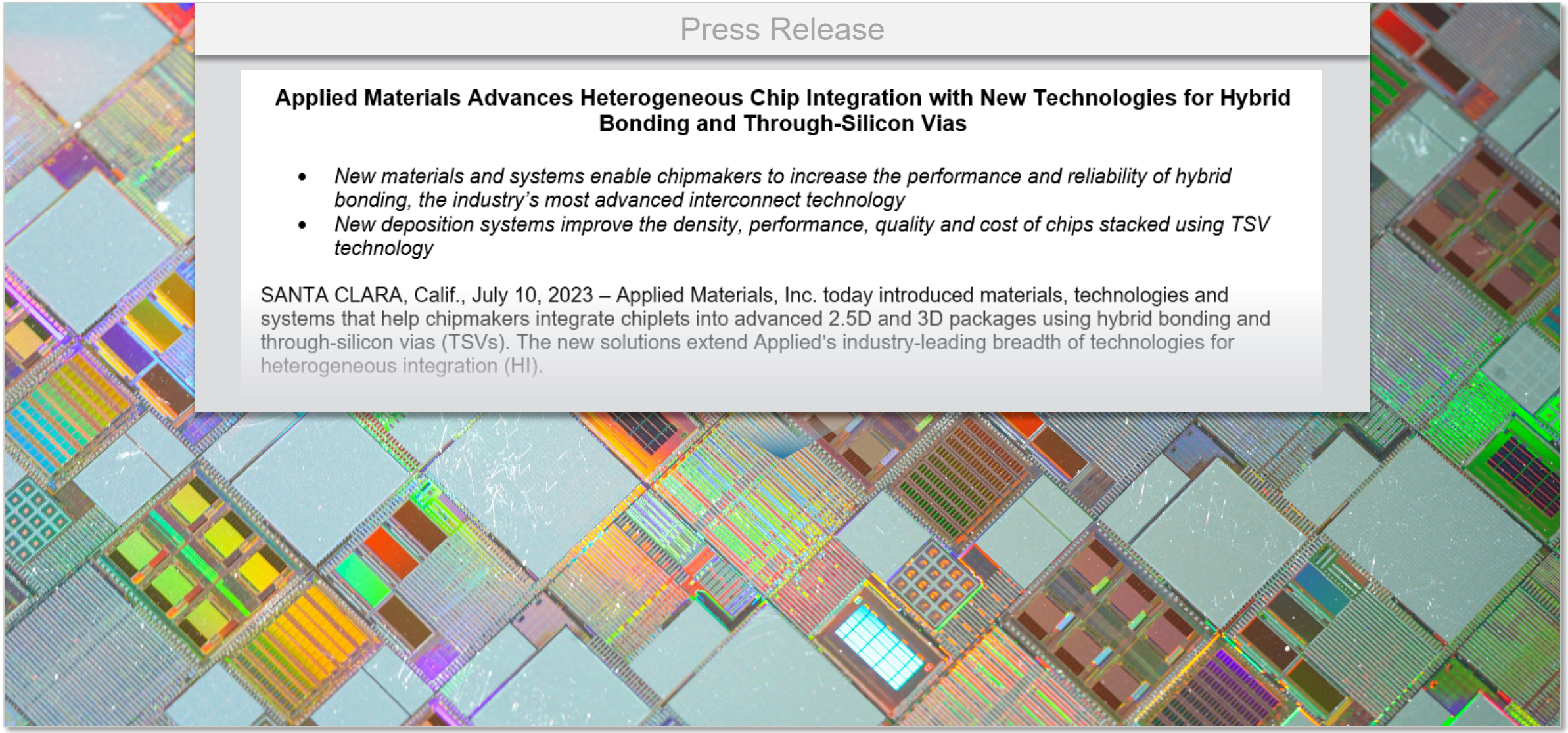


Source: Li et al., IRPS (2016); Agrawal et al., ECTC (2017); Gao et al,, ECTC (2021)



APPLIED MATERIALS

New Products Enable Heterogeneous Integration



Press Release

Applied Materials Advances Heterogeneous Chip Integration with New Technologies for Hybrid Bonding and Through-Silicon Vias

- *New materials and systems enable chipmakers to increase the performance and reliability of hybrid bonding, the industry's most advanced interconnect technology*
- *New deposition systems improve the density, performance, quality and cost of chips stacked using TSV technology*

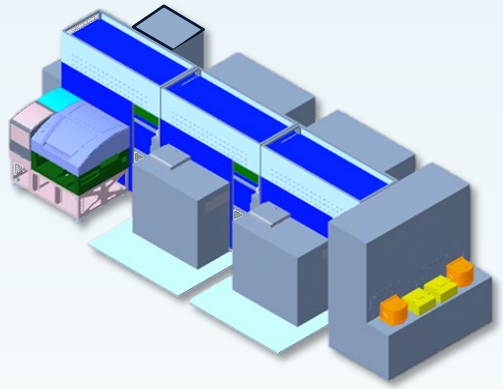
SANTA CLARA, Calif., July 10, 2023 – Applied Materials, Inc. today introduced materials, technologies and systems that help chipmakers integrate chiplets into advanced 2.5D and 3D packages using hybrid bonding and through-silicon vias (TSVs). The new solutions extend Applied's industry-leading breadth of technologies for heterogeneous integration (HI).

Key Playbook Elements for Heterogenous Integration

Innovating how we innovate

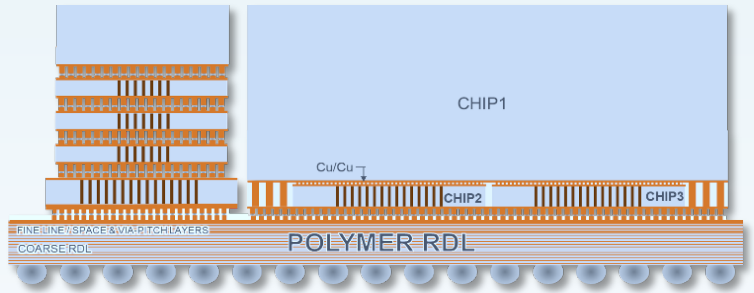
Advanced Packaging Development Center for Heterogeneous Integration

New products for integrated processes



Integrated Materials Solution® for Die-to-Wafer Hybrid Bonding

System level innovations for PPACt™ acceleration



Industry Enablement of 2.5D and 3D IC Packaging Solutions

Heterogenous Integration Panel

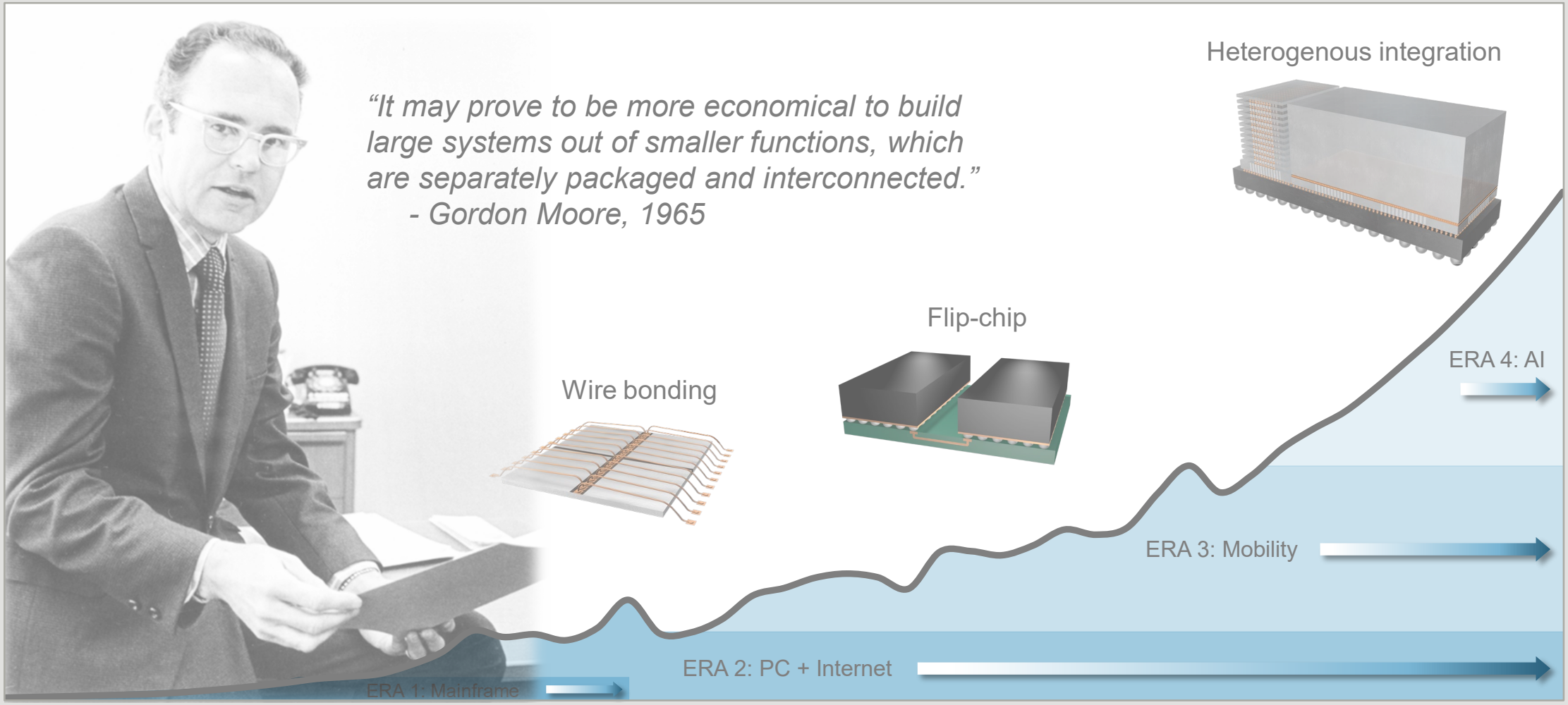
Vincent DiCaprio

Vice President, Business and Corporate Development

Heterogeneous Integration and ICAPS

Semiconductor Products Group

Heterogeneous Chip Design – An Evolution of Moore's Law



Source: SEMI, VLSI, Applied Materials https://archive.computerhistory.org/resources/access/text/2017/03/102770822-05-01-acc.pdf

PC: Personal Computer
AI: Artificial Intelligence

Heterogenous Integration Panel

Mark Fuselier

SVP of Technology and Product Engineering

AMD

Babak Sabi

SVP of Assembly Test Technology Development

Intel

PR "Chidi" Chidambaram

VP of Engineering

Qualcomm

Richard Blickman

Founder and CEO

Besi

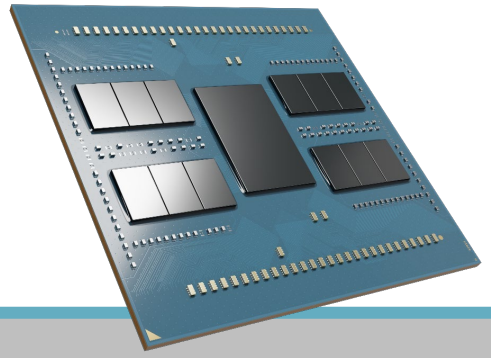
Paul Lindner

Executive Technology Director

EV Group

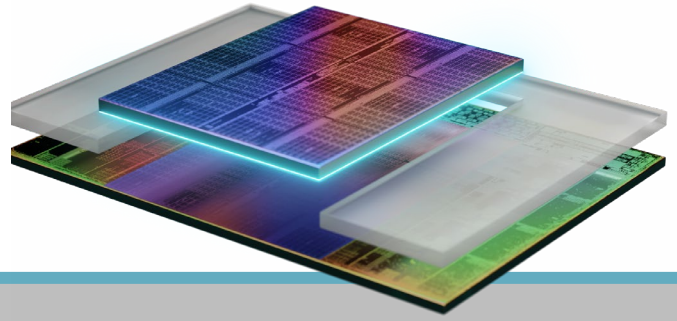
Enabling Faster Scale of Compute Capability

AMD
together we advance_



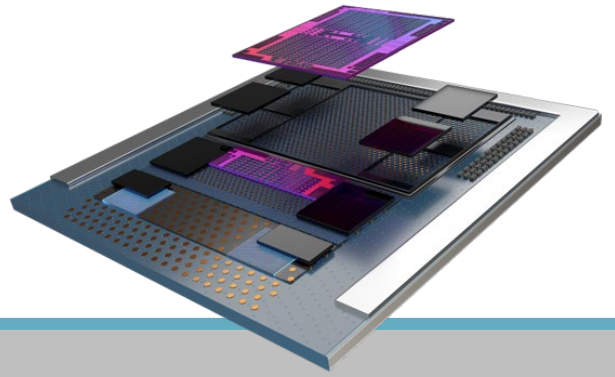
Cost & Time to Market

- 2nd/3rd/4th Gen EPYC™
  - Separate I/O chiplet
  - CPU in latest technology gen
  - Infinity fabric for die-to-die interconnect



Memory Integration

- 2.5D GPU with HBM
  - Interposer/TSV interconnectivity
- 3D Stacking
  - Added last level cache density by stacking memory & CPU



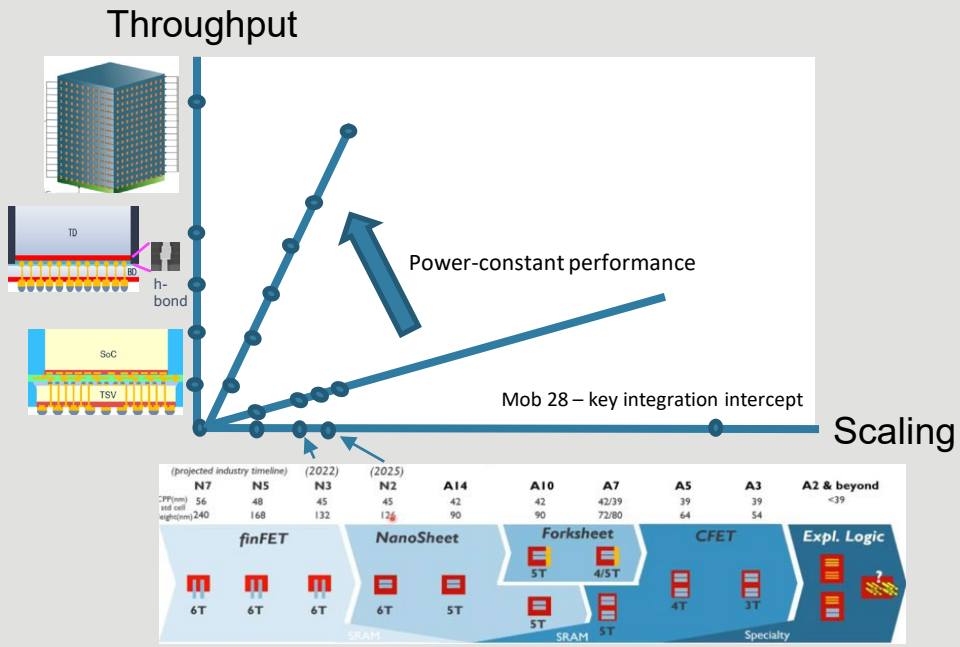
Heterogenous SoC

- 3D & 2.5D integration
  - CPU, GPU & HBM in single module
  - Designed to improve Perf/W and TCO for AI workloads

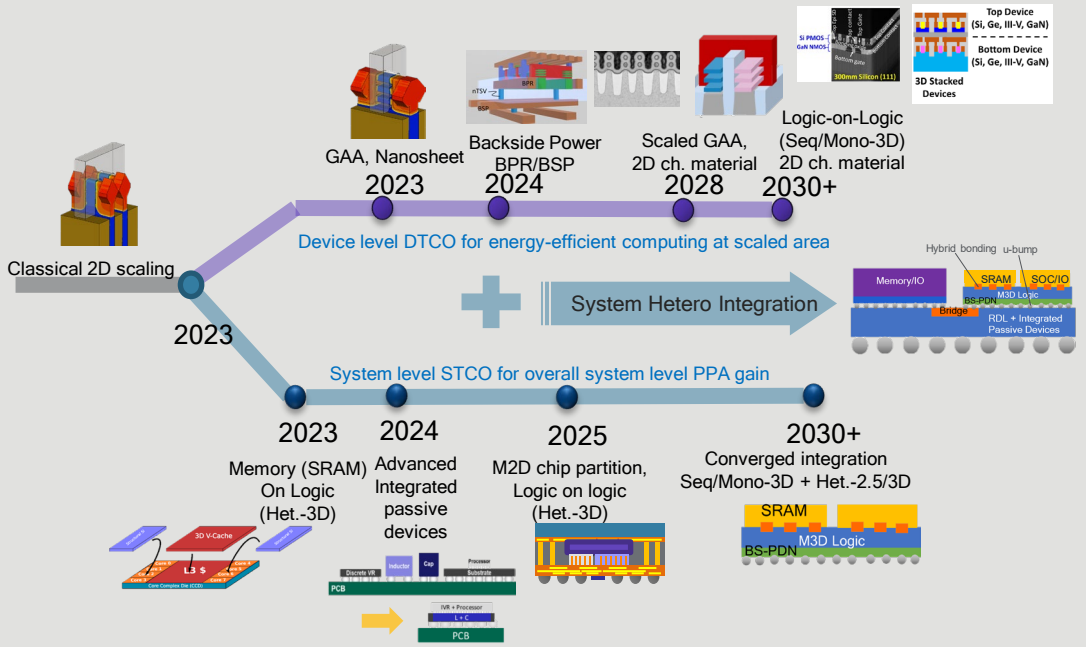
Evolution of the Heterogeneous Roadmap

Qualcomm

Today: Integration augments scaling

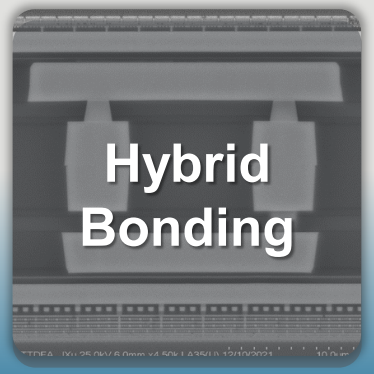


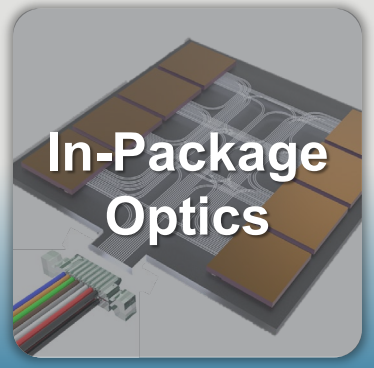
Tomorrow: Tech node coupled with integration



Vision of the Future for AI/HPC

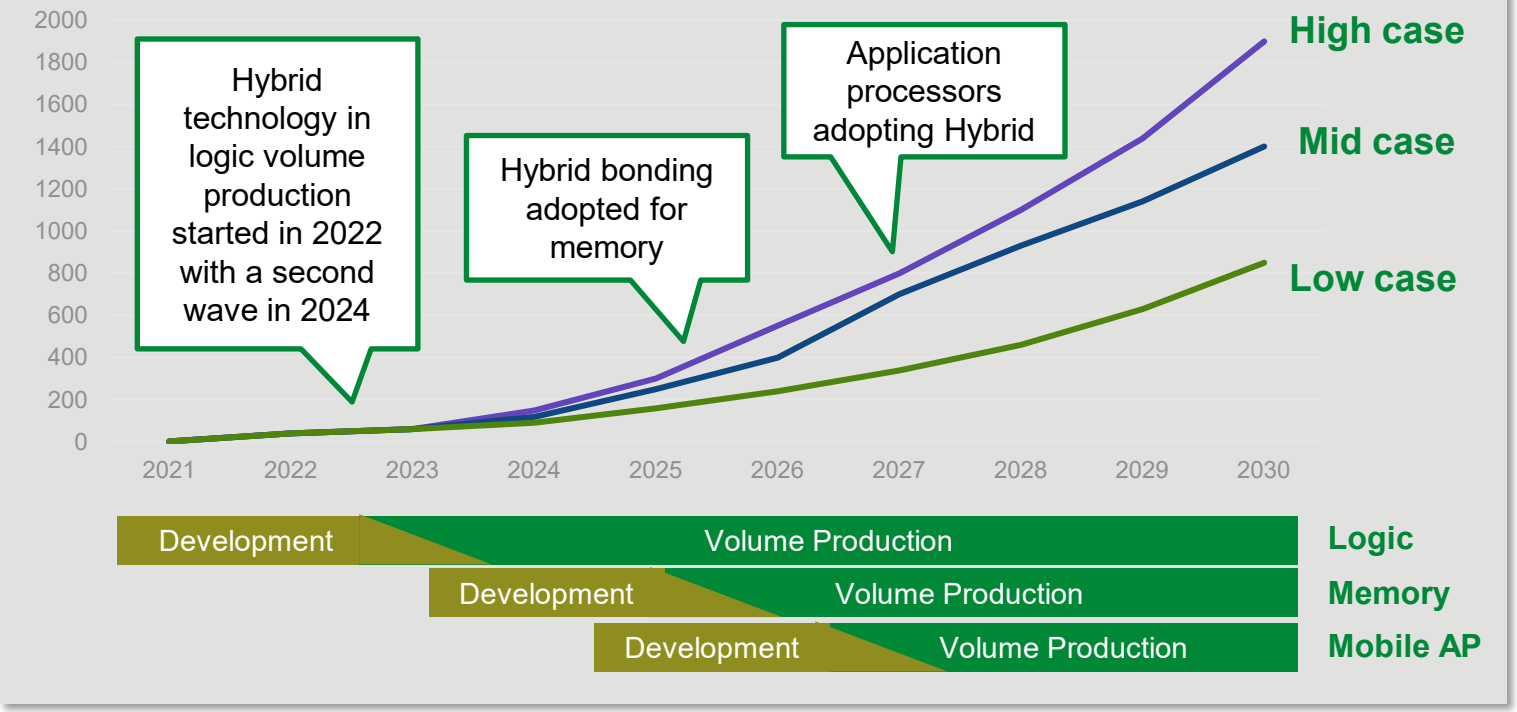
Advanced packaging enables high density interconnects with larger die complexes from multiple process nodes





Core count & uncore scaling limitations	On- and off-package latency in large die complexes	Memory partitioning local vs pooled	Performance per socket drives massive die complexes

Estimated Hybrid Bonding Market Development



Estimated 800 – 1,900 systems cumulative by 2030

- Logic device production and adoption continues
- Technology adoption coming in waves
- Major memory companies engaged
  - Starting programs for HBM4 Hybrid packages
- Increased interest for HB usage in consumer applications

Changes to market forecast vs. CMD ’22

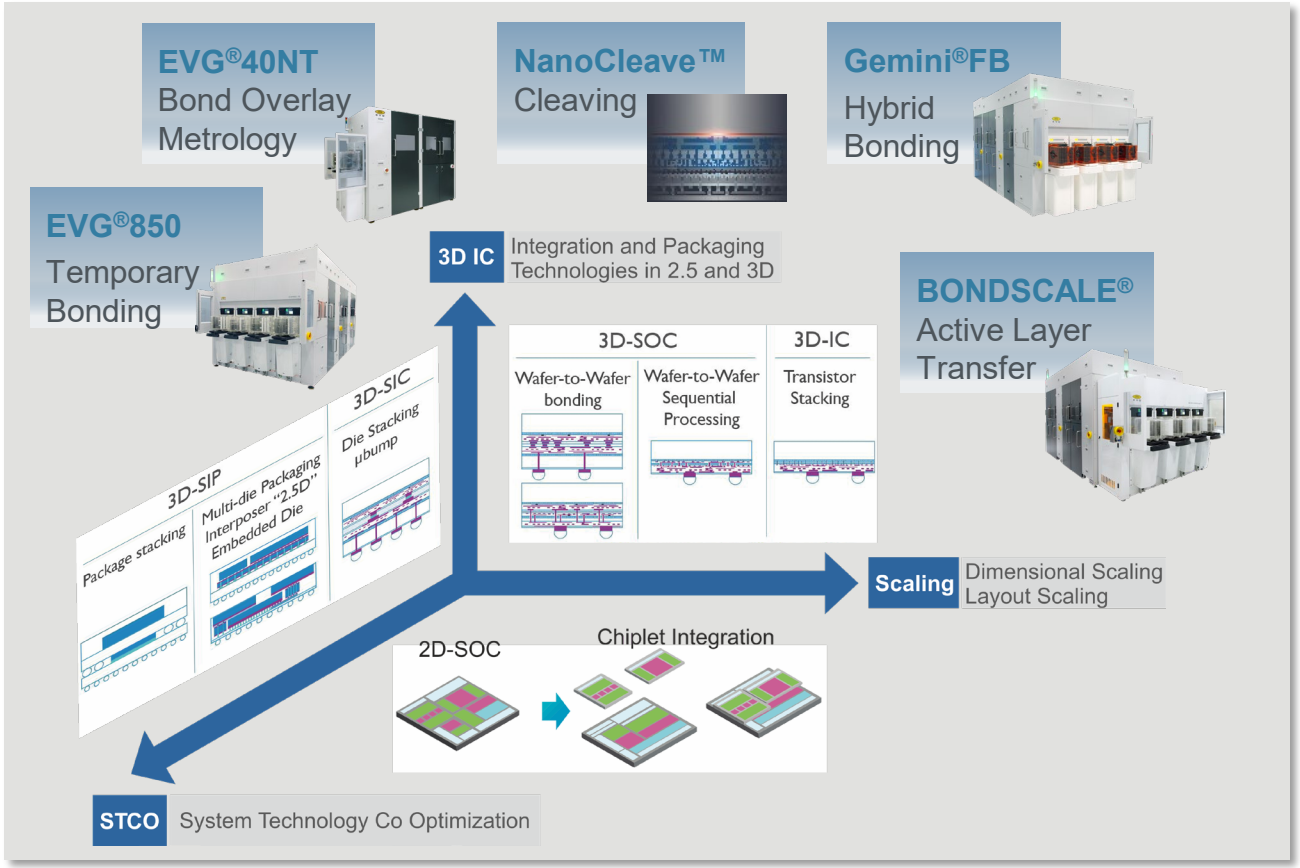
- Upside and low case unit potential expanded
- Tracking to mid case currently
- Higher ASPs anticipated due to higher accuracy requirements post 2024

Expected rollout sequence:

- Logic
- Memory
- Mobile
- Other Applications

Source: Besi estimates, June 2023
Cases based on potential adoption scenarios

Wafer Bonding is a Scaling Booster



- Wafer Bonding
  - » Complements the traditional dimensional scaling
- Wafer-to-Wafer Hybrid Bonding:
  - » Enables higher functional density at the wafer level back end
- Active Layer Transfer Fusion Bonding:
  - » Exploits the wafer back side and enables front end transistor level stacking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MATERIALS®
make possible