

Applied Materials Sees Innovation and Industry Collaboration as Vital to Keeping Moore's Law Alive

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SANTA CLARA, Calif.--(BUSINESS WIRE)--Jul. 14, 2009-- While the current economic environment is imposing severe constraints on the semiconductor equipment industry, the primary driver for increasing profitability for leading-edge chipmakers is still Moore's Law. However, moving to the next technology node will require even higher levels of R&D investment to overcome key technical barriers. The semiconductor equipment industry must find ways to make today's reduced R&D budgets meet these challenges.

"The current size of the wafer fabrication equipment industry does not support the significant levels of R&D spending needed to follow Moore's Law and deliver leading-edge systems and processes to customers. This is becoming an increasingly evident as logic, DRAM and flash technologies continue to diverge," said Tom St. Dennis, senior vice president and general manager of Applied's Silicon Systems Group. "To support our customers in advancing their technology roadmaps and provide critical customer services, we see the need for new business models and alliances to optimize the utilization of our industry's resources."

At SEMICON West in San Francisco this week, Applied Materials, Inc. will focus on the strategies and technologies that will be needed for the semiconductor industry to successfully navigate these challenging times. In an important ITRS keynote panel on July 15, moderated by George Scalise, president of the SIA, St. Dennis will join a panel of experts representing a cross-section of the industry who will explore the impact of business model shifts on "the Future of Innovation."

Tom St. Dennis will also be featured at SEMI's press luncheon panel on July 14 where he will provide insights into how the macroeconomic environment, market drivers and cleantech are influencing the pace and direction of R&D in semiconductor technology.

At SEMI's popular TechXPOT seminars, Applied will present key strategies from three-dimensional (3-D) TSV* chip packaging to cutting-edge unit process technologies. 3-D IC integration is a new way for chip designers to deliver higher density, lower power consumption devices without necessarily scaling the technology node. Find out how Applied and other equipment suppliers are working together to enable the cost-effective adoption of this exciting technology.

Applied's technologists will also share the latest advances in fabrication technology, including novel epitaxial processes for boosting transistor performance and innovations to extend PVD technology to the 22nm node and beyond without employing risky new integration schemes. For a complete schedule of Applied's participation in the SEMICON West technical program, visit www.appliedmaterials.com/about/events.html.

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*TSV=through silicon via

Source: Applied Materials, Inc.

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